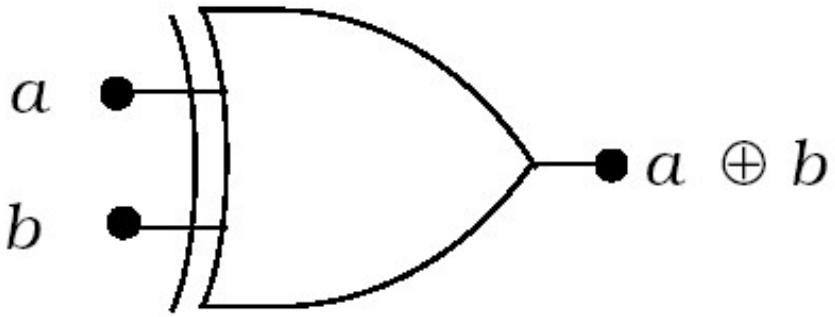
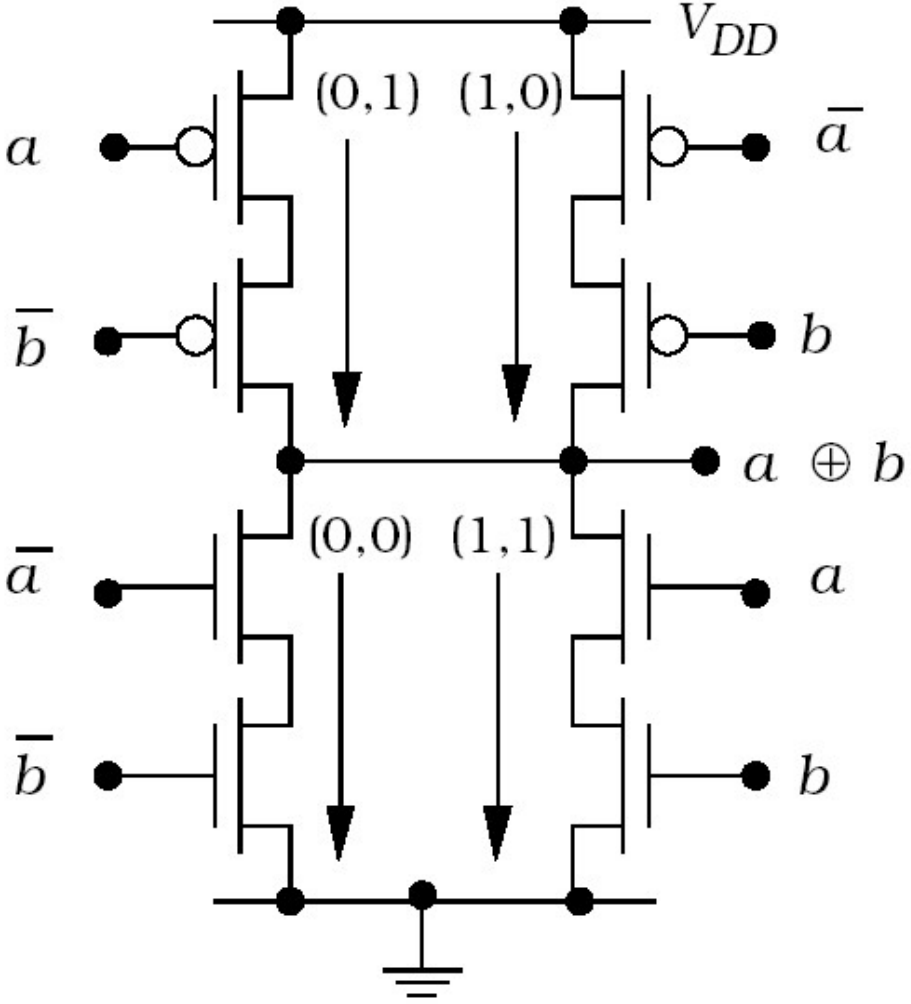
Introduction to VLSI Circuits and Systems by J. Uyemura, Wiley, 2002, ISBN-10: 0-471-12704-3.

All figures are from this book.

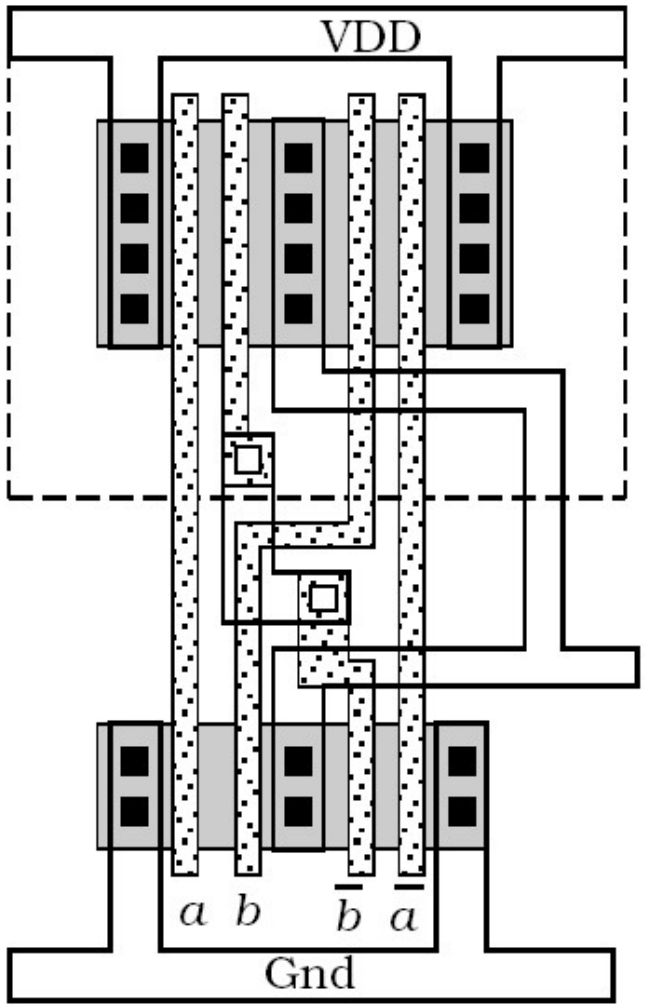


a	b	$a \oplus b$	On devices
0	0	0	nFET
0	1	1	pFET
1	0	1	pFET
1	1	0	nFET

Figure 9.1 (p. 339)
XOR function table.



(a) Circuit



(b) Layout

Figure 9.2 (p. 340)
XOR mirror circuit.

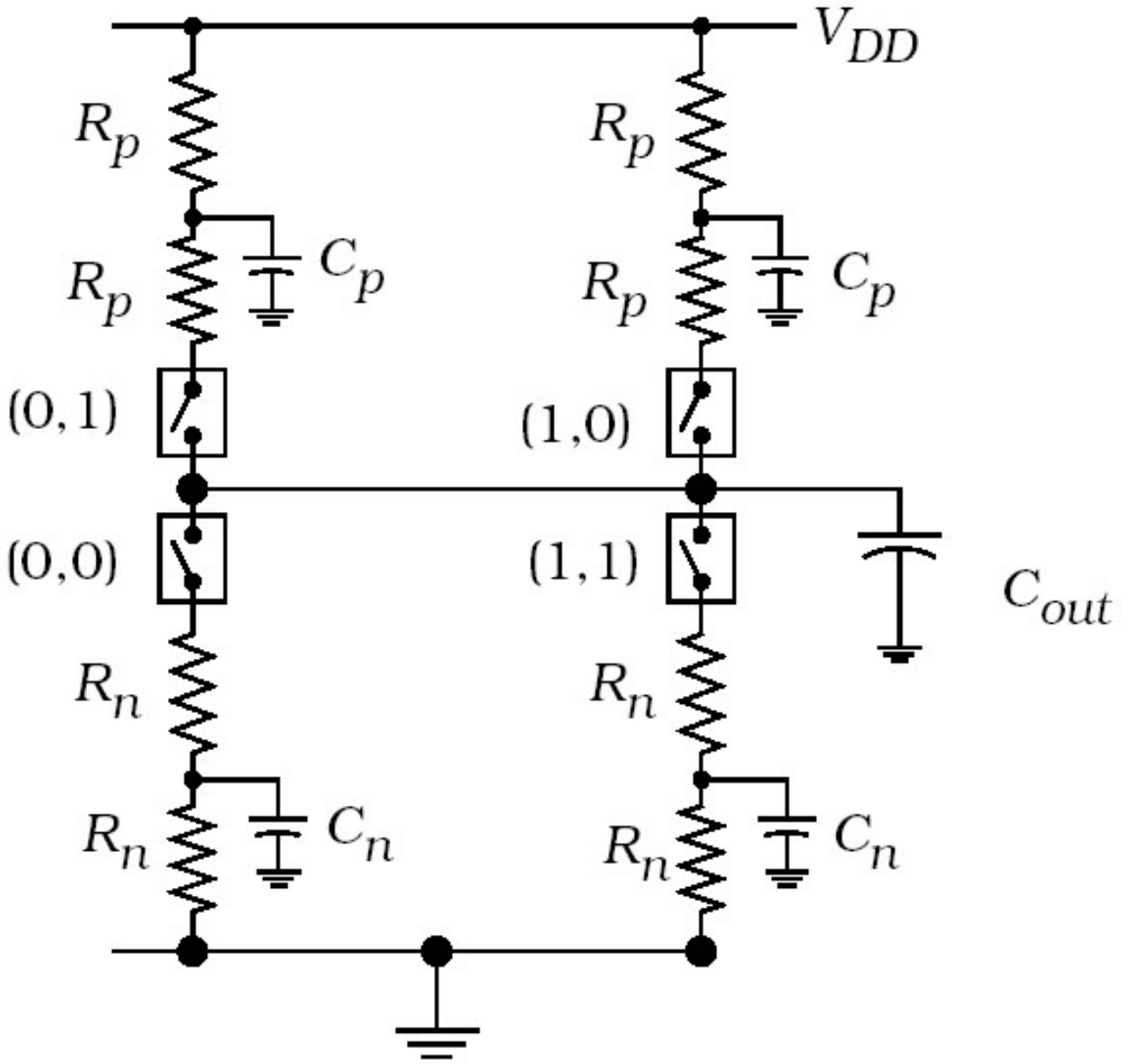
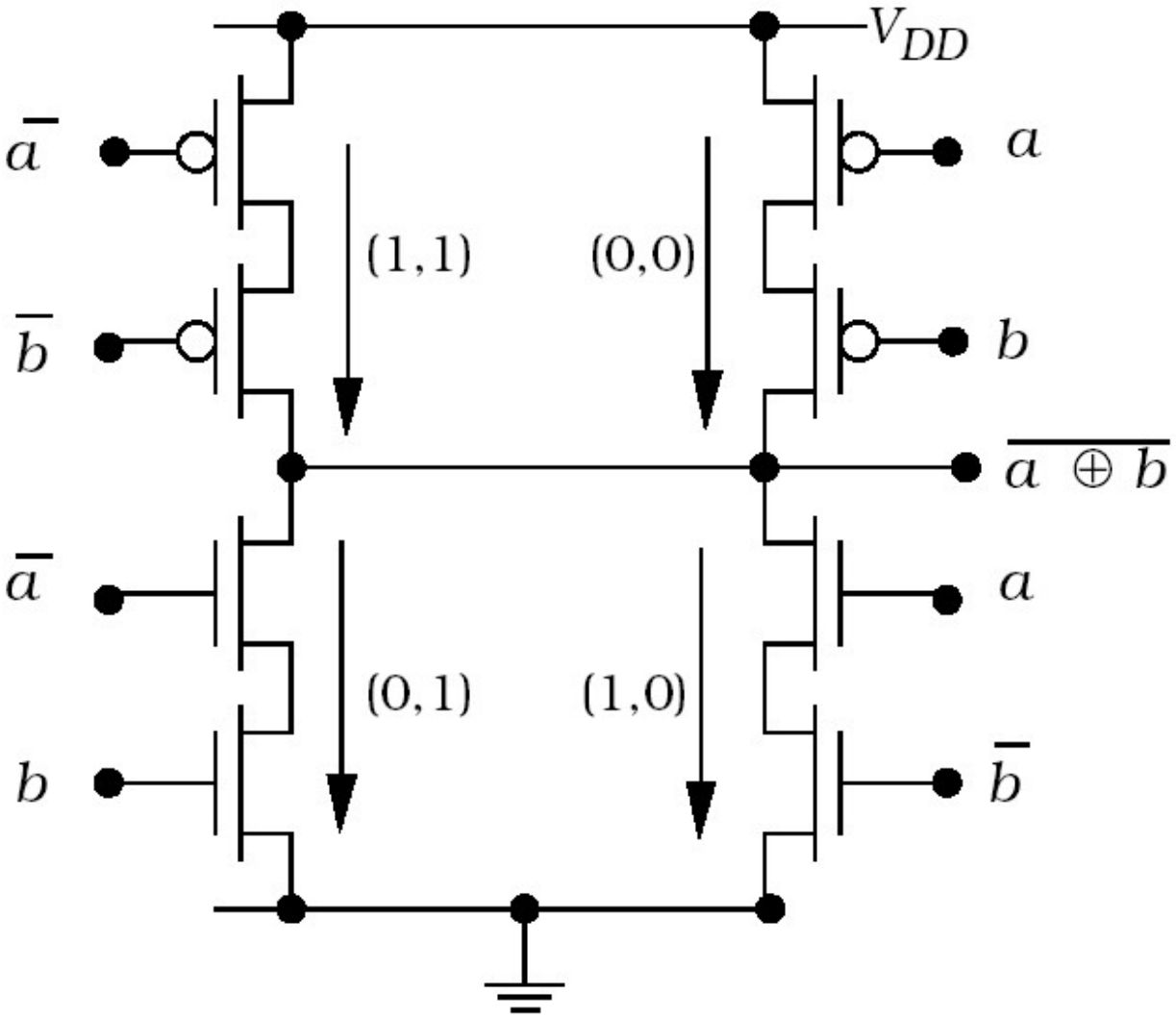


Figure 9.3 (p. 341)
Switch model for transient calculations.



a	b	$\overline{a \oplus b}$
0	0	1
0	1	0
1	0	0
1	1	1

Figure 9.4 (p. 341)
Exclusive-NOR (XNOR) mirror circuit.

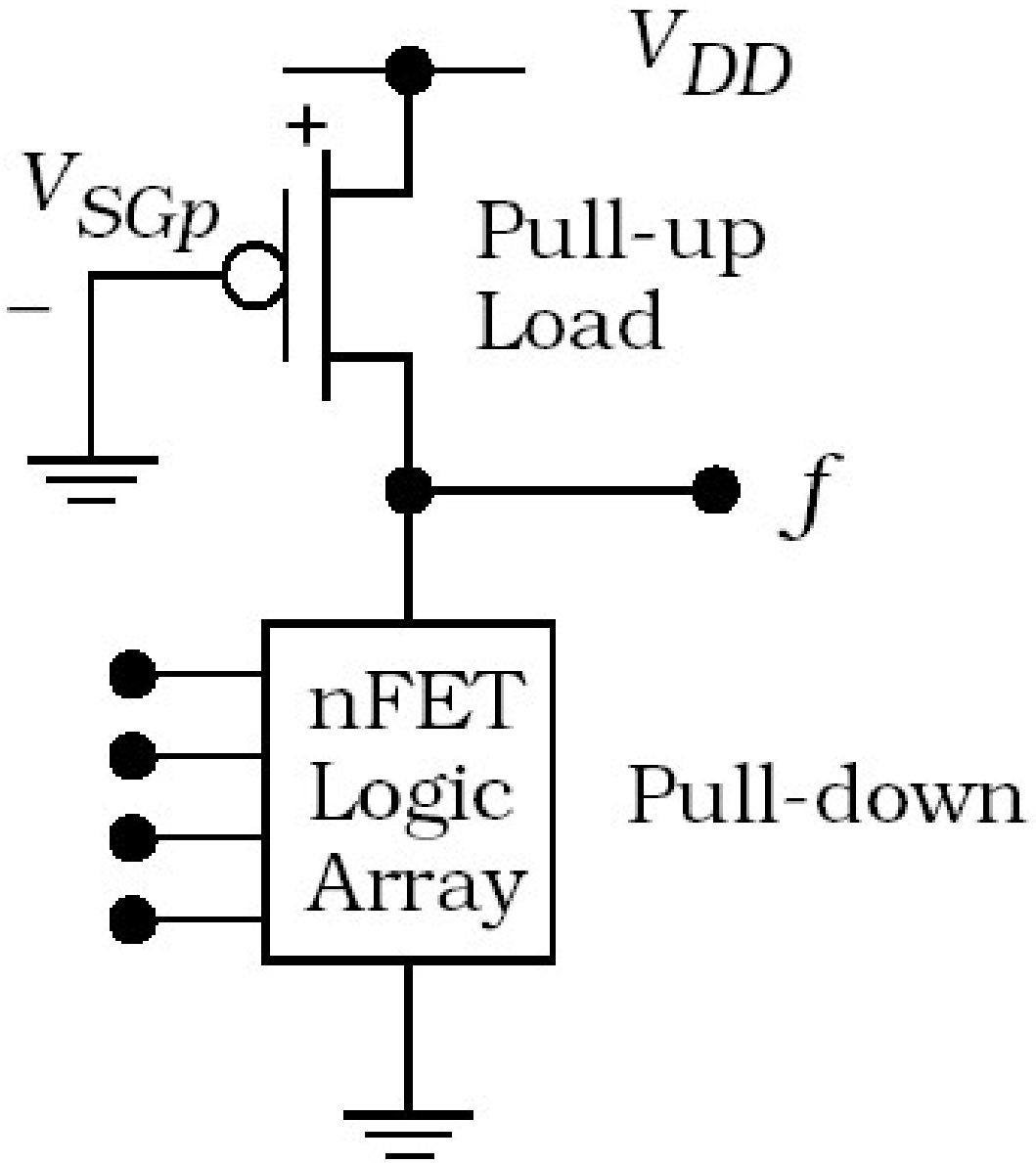


Figure 9.5 (p. 342)
General structure of a pseudo-nMOS logic gate.

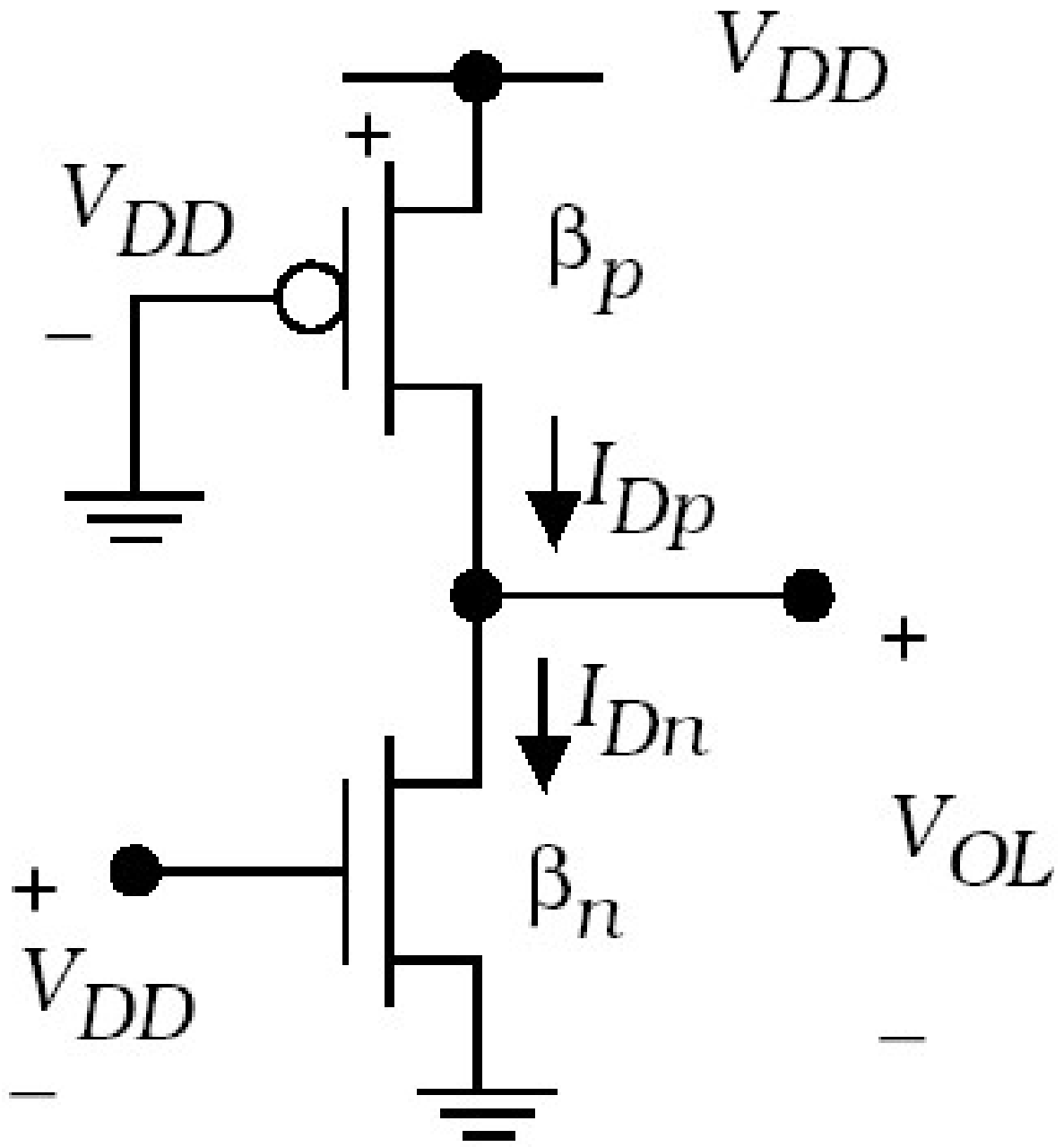


Figure 9.6 (p. 343)
Pseudo-nMOS inverter.

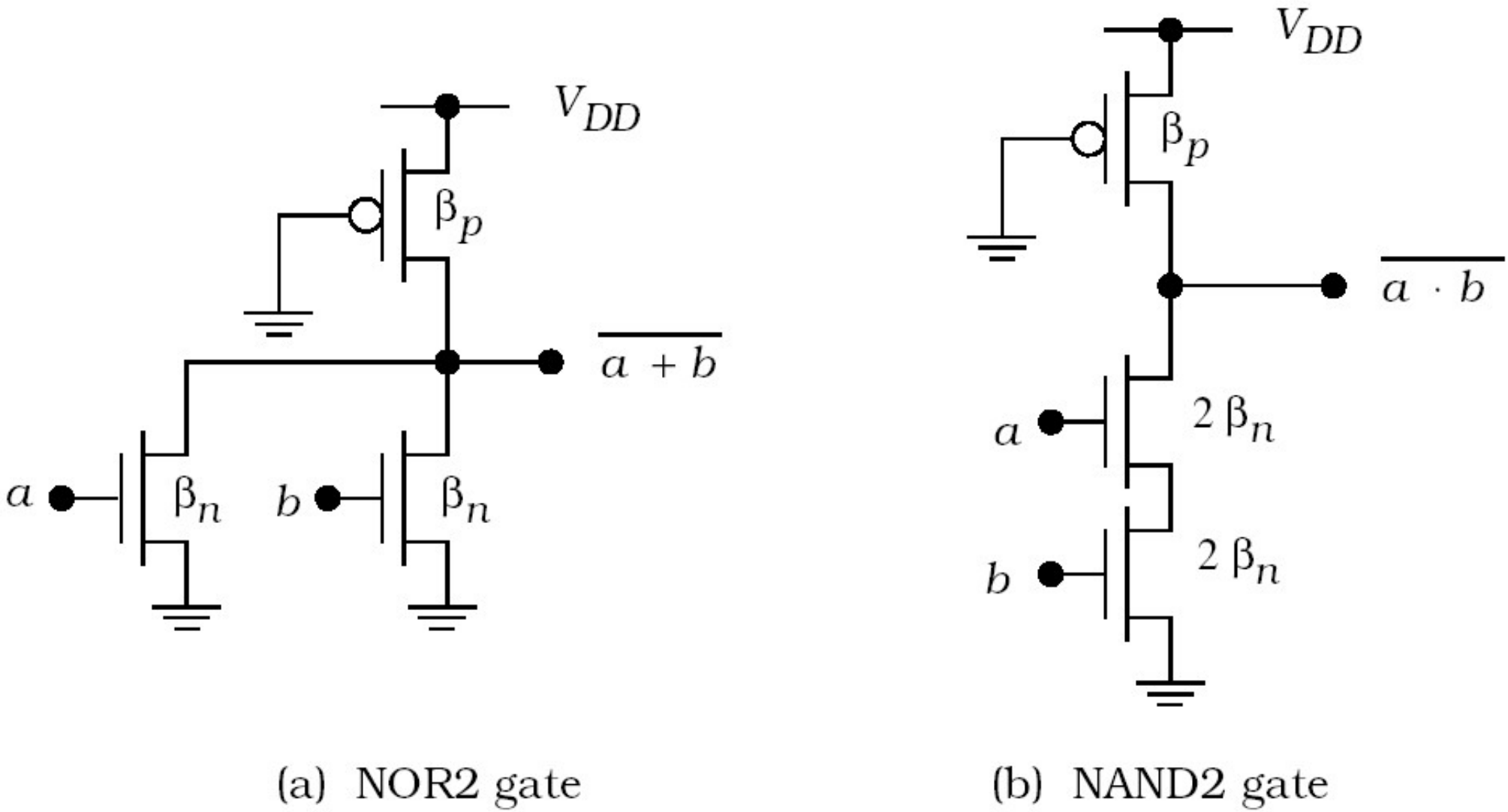
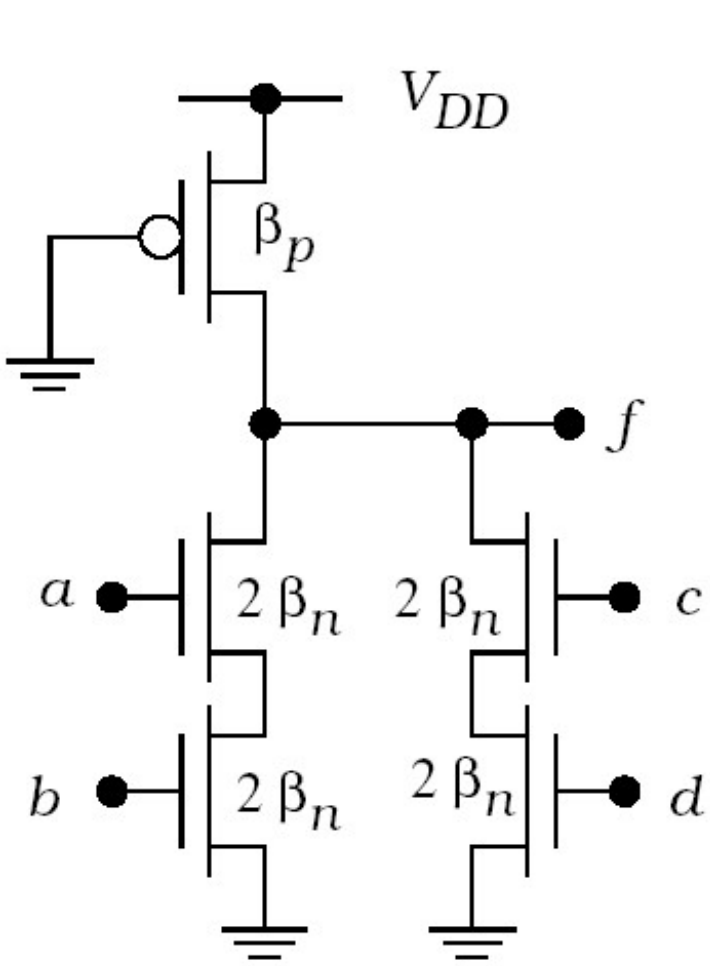
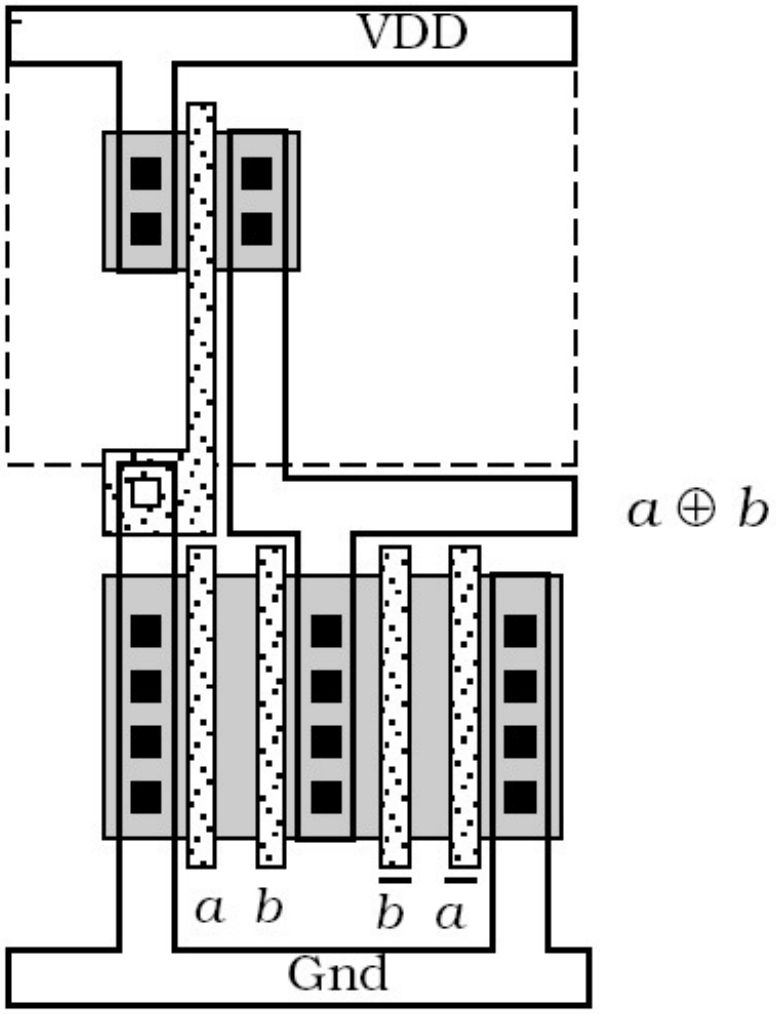


Figure 9.7 (p. 344)
Pseudo-nMOS NOR and NAND gates.

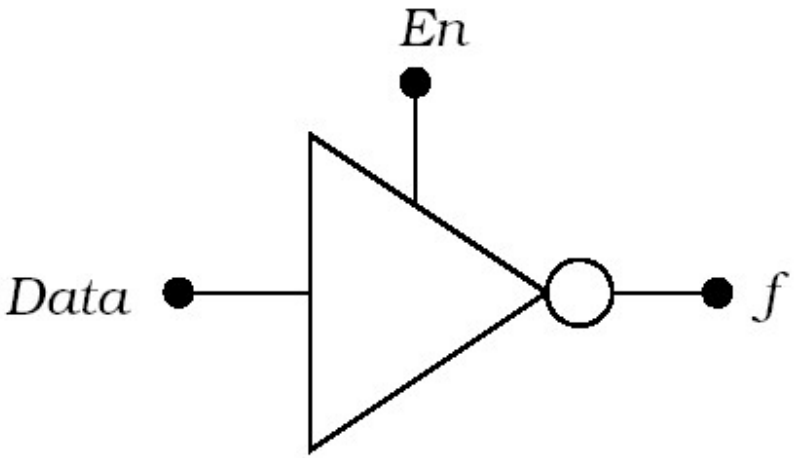


(a) General circuit



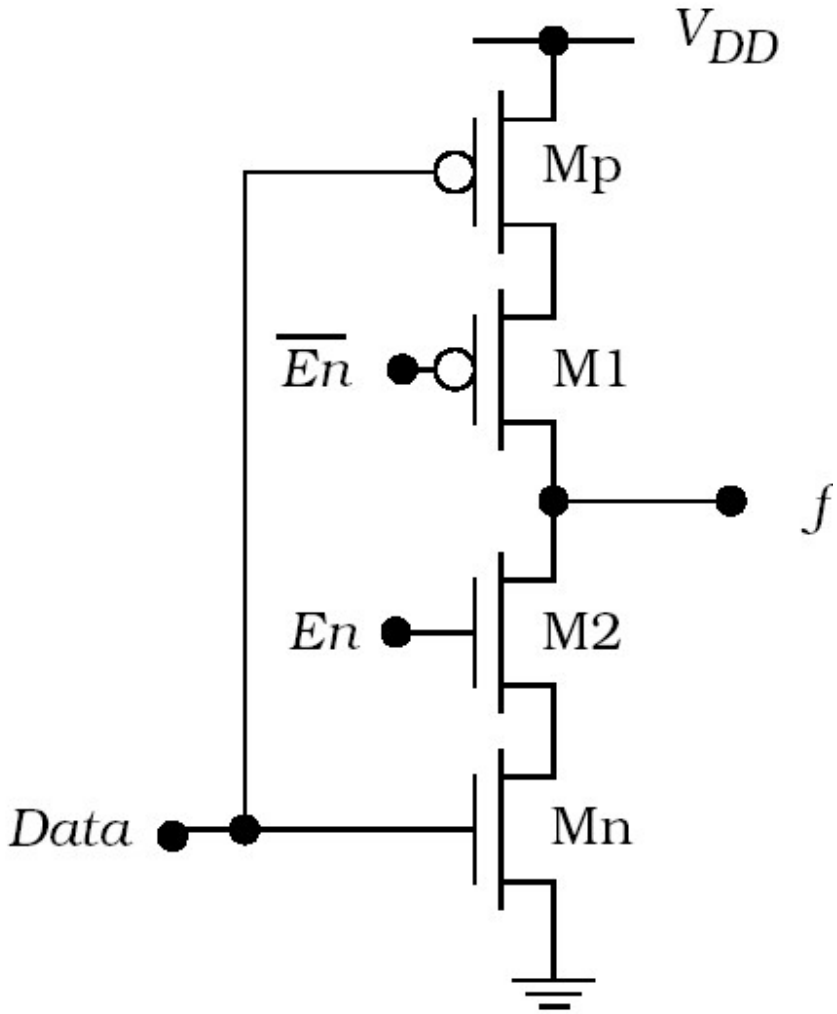
(b) Layout example

Figure 9.8 (p. 345)
AOI gate in pseudo-nMOS logic.



En	f
0	Z
1	$\overline{Data}$

(a) Symbol and operation



(b) CMOS circuit

Figure 9.9 (p. 345)
Tri-state inverter.

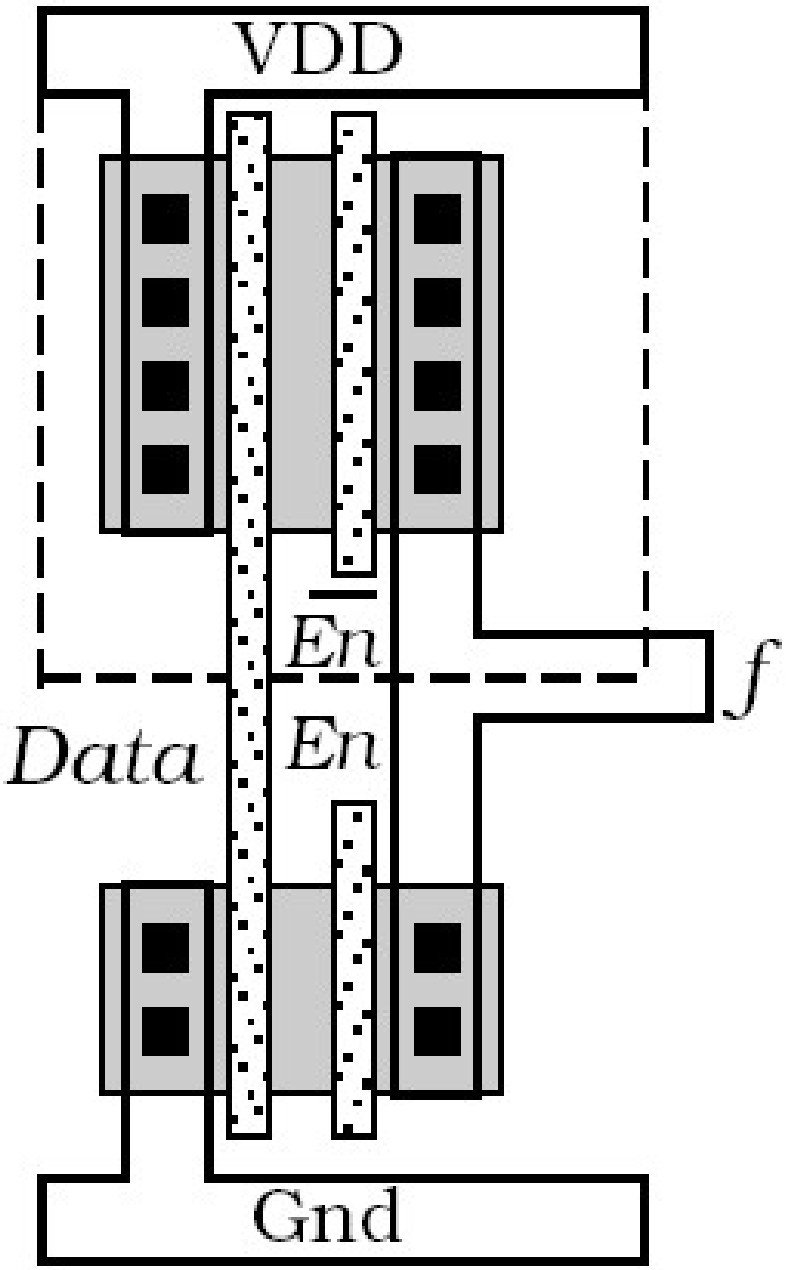


Figure 9.10 (p. 346)
Tri-state layout.

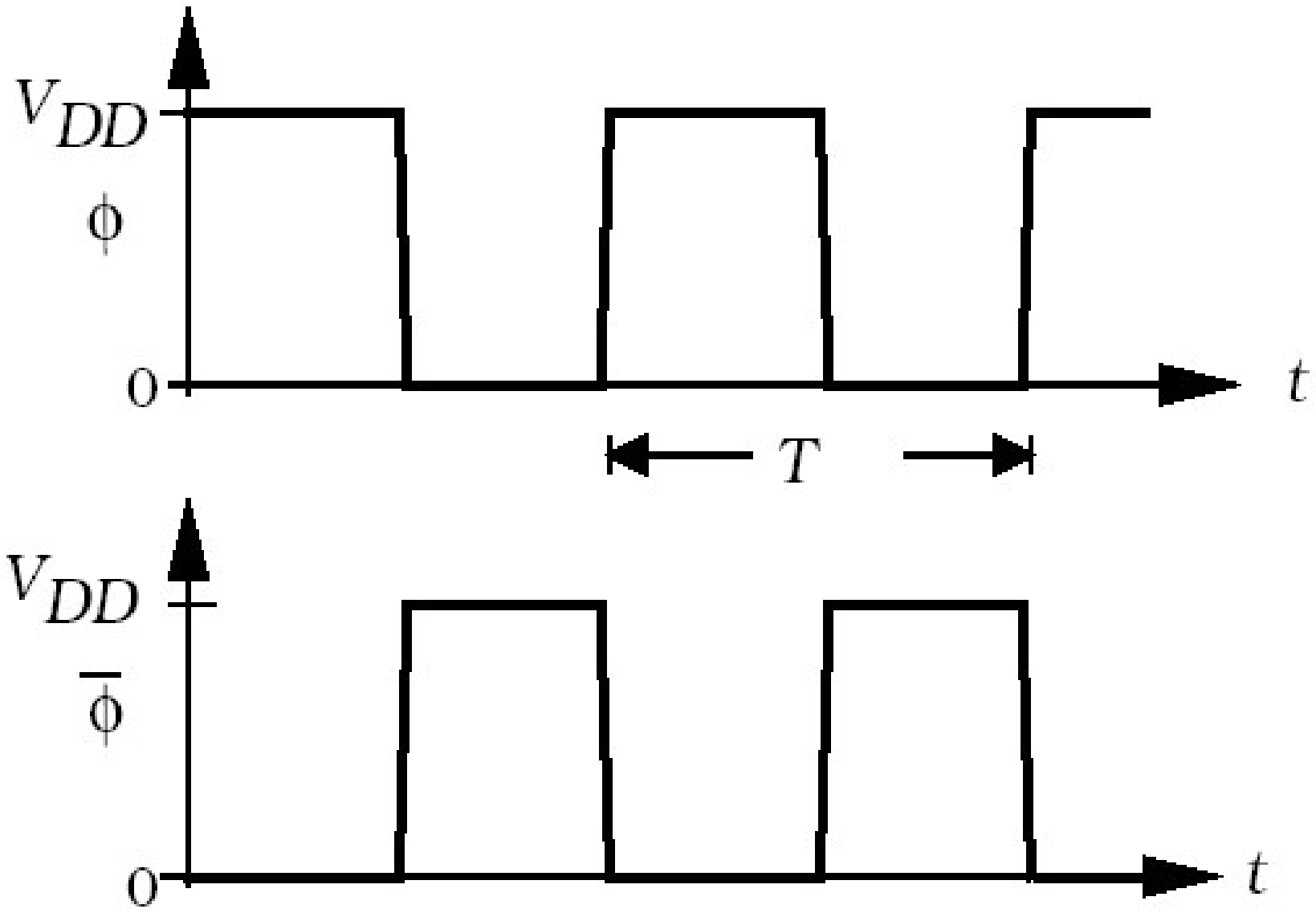
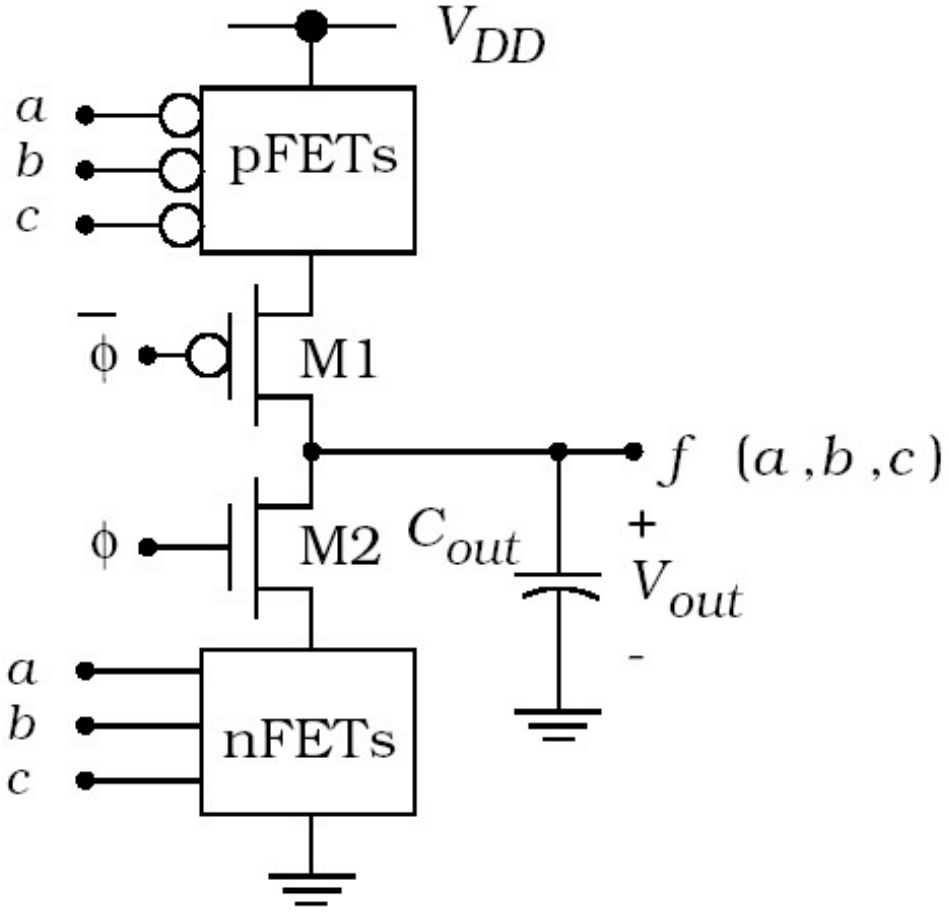


Figure 9.11 (p. 347)
Clocking signals.



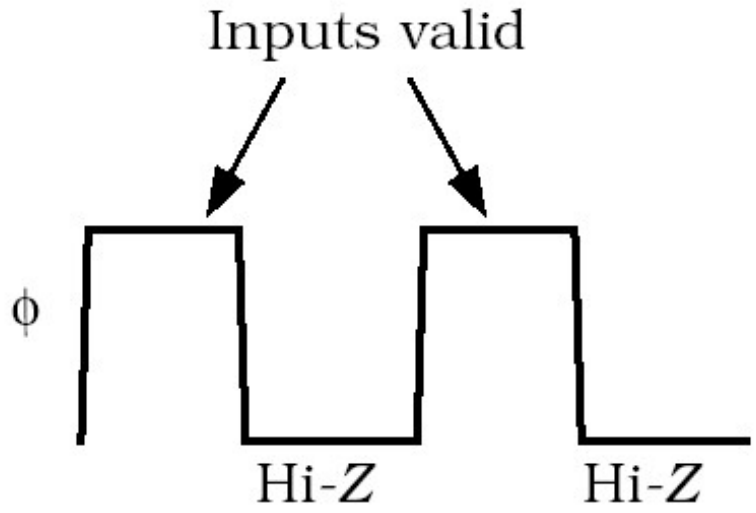
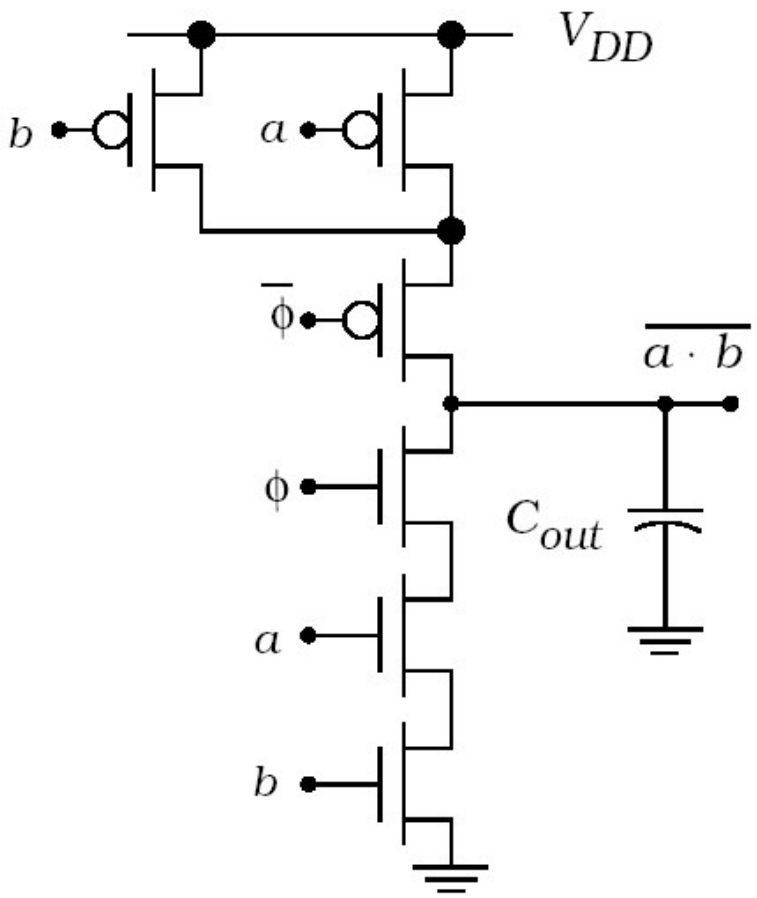
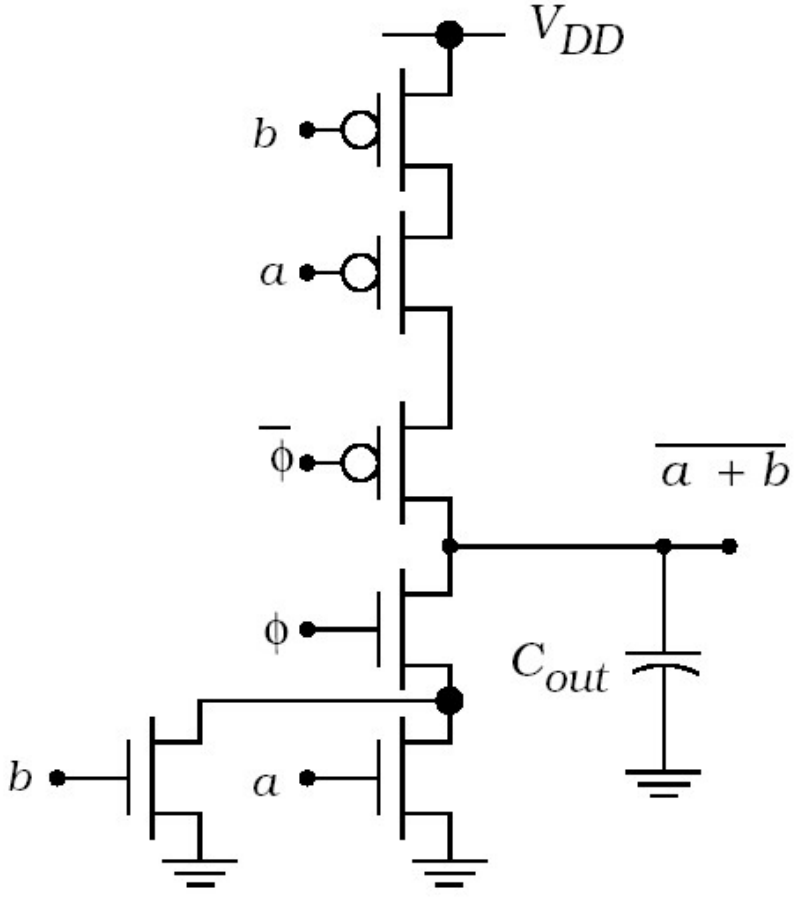


Figure 9.12 (p. 347)
Structure of a C²MOS gate.



(a) NAND2 circuit



(b) NOR2 circuit

Figure 9.13 (p. 348)
Example of clocked-CMOS logic gates.

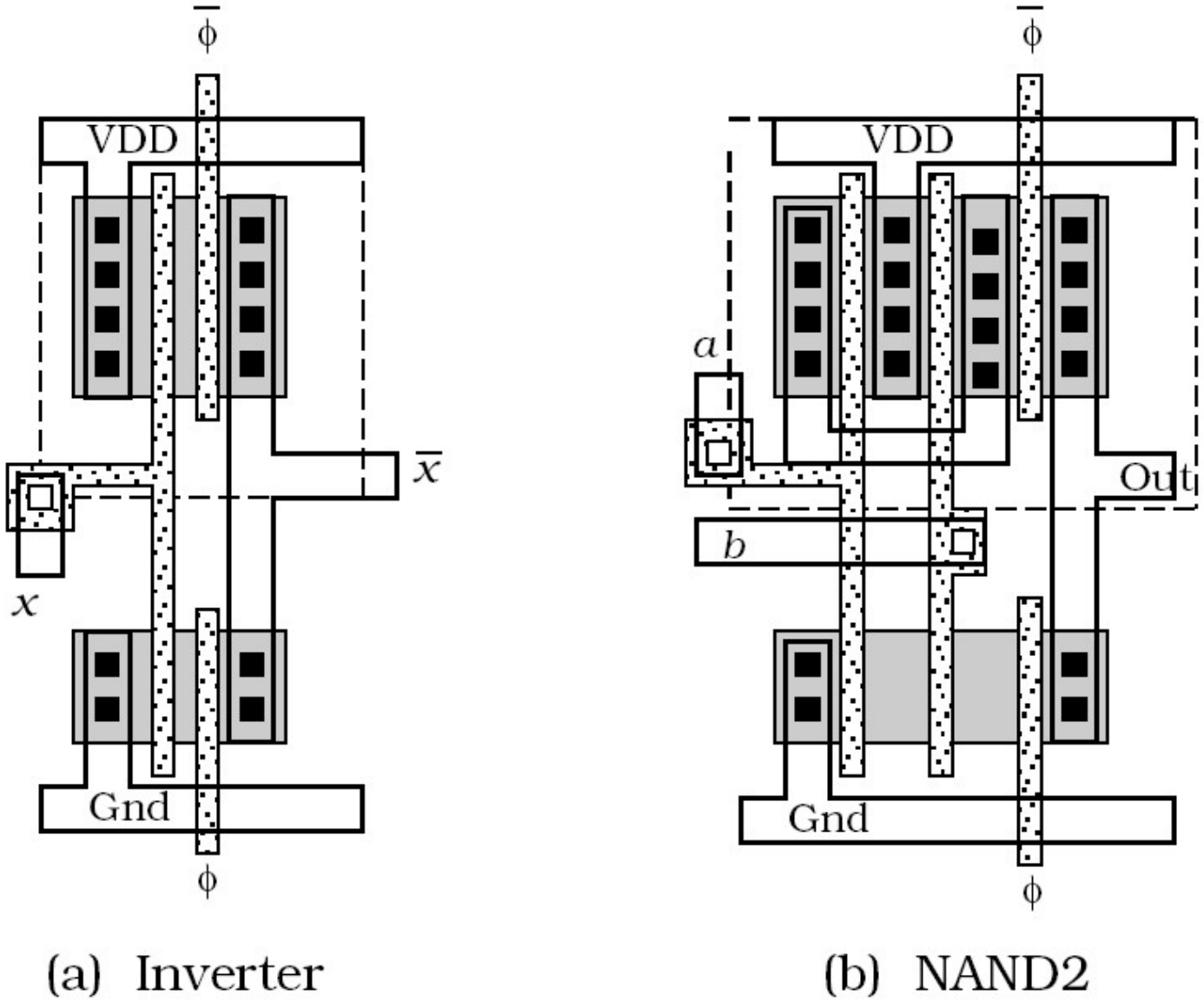
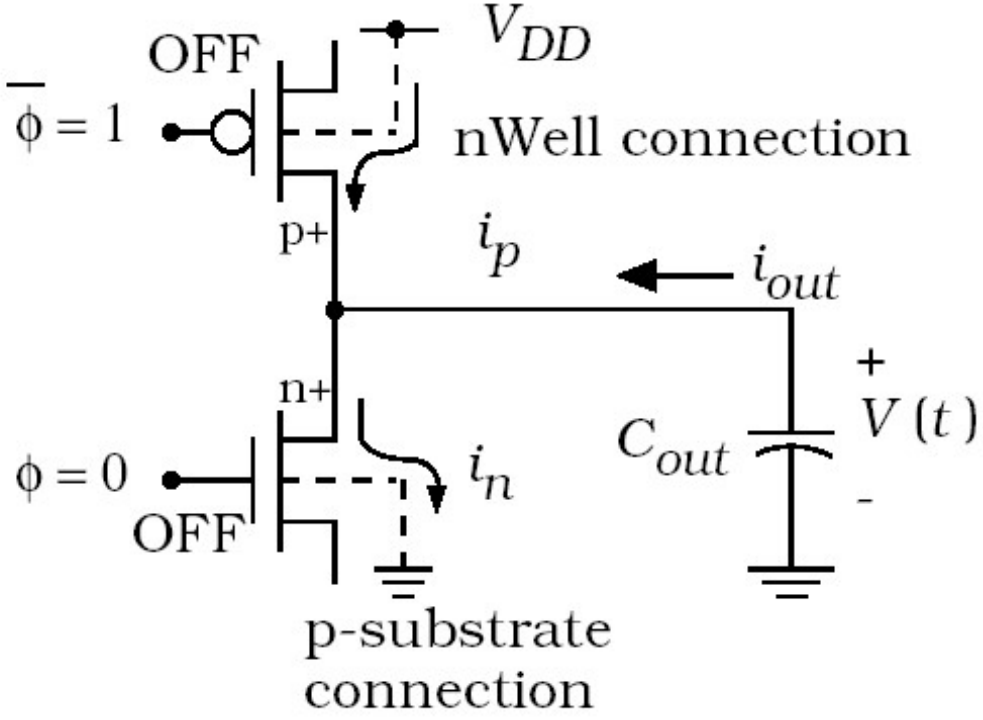
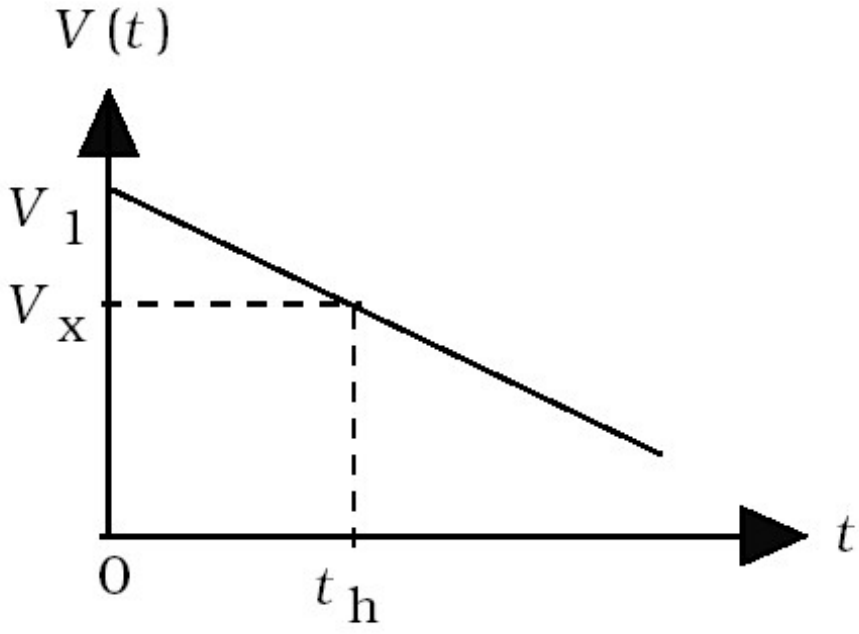


Figure 9.14 (p. 348)
Layout examples of C^2MOS circuits.



(a) Bulk leakage currents



(b) Logic 1 voltage decay

Figure 9.15 (p. 349)
Charge leakage problem.

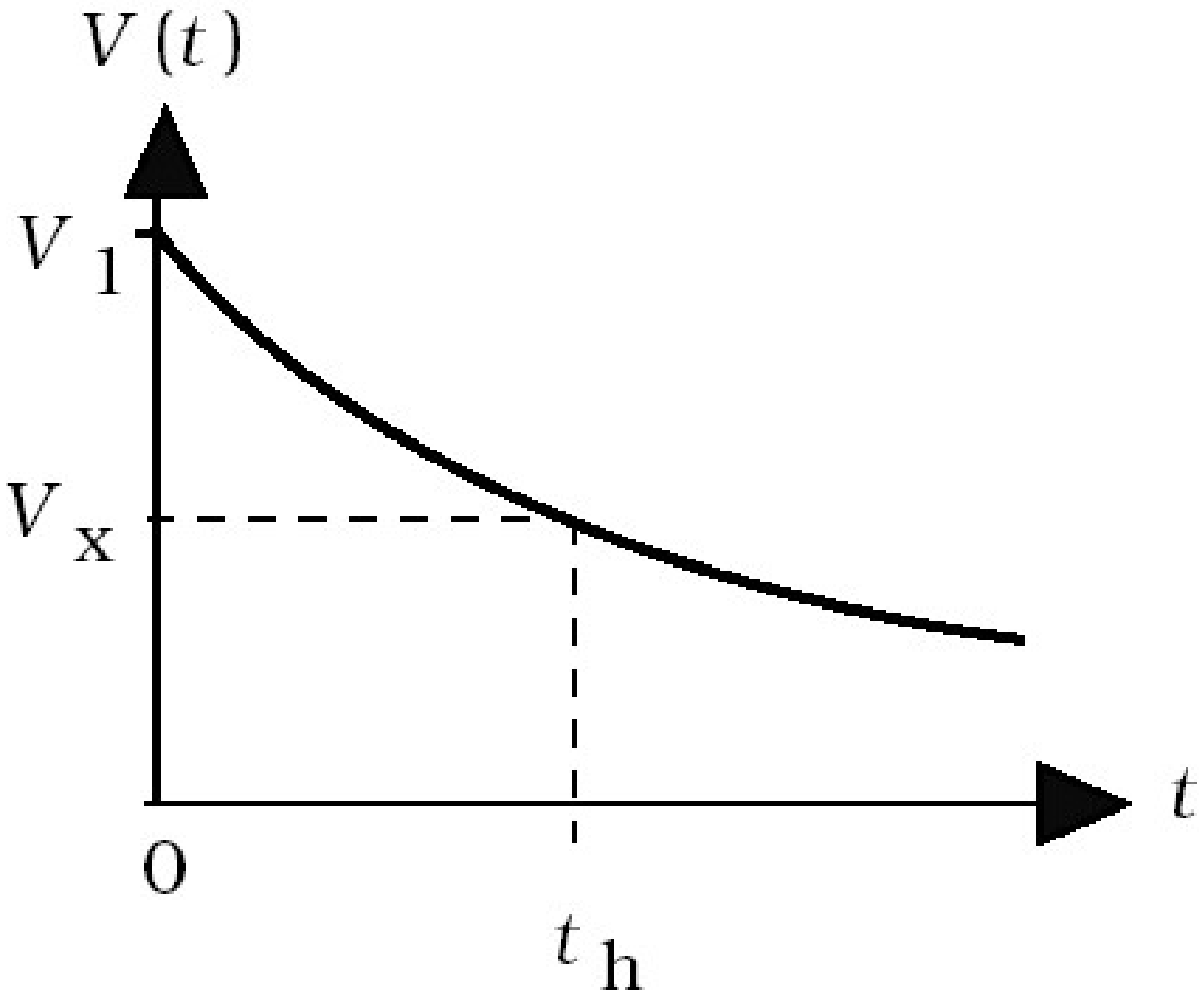
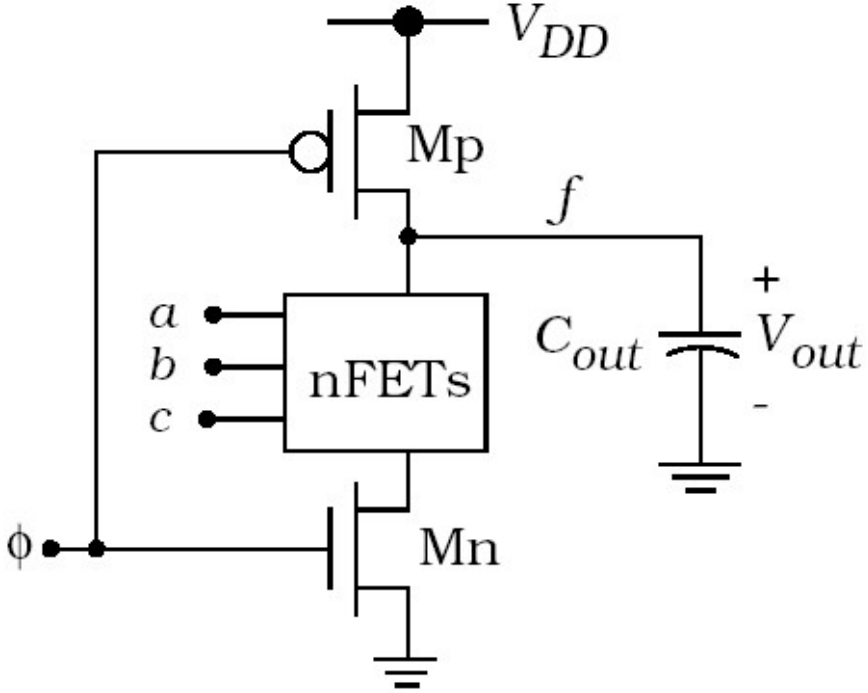


Figure 9.16 (p. 352)
General voltage decay.



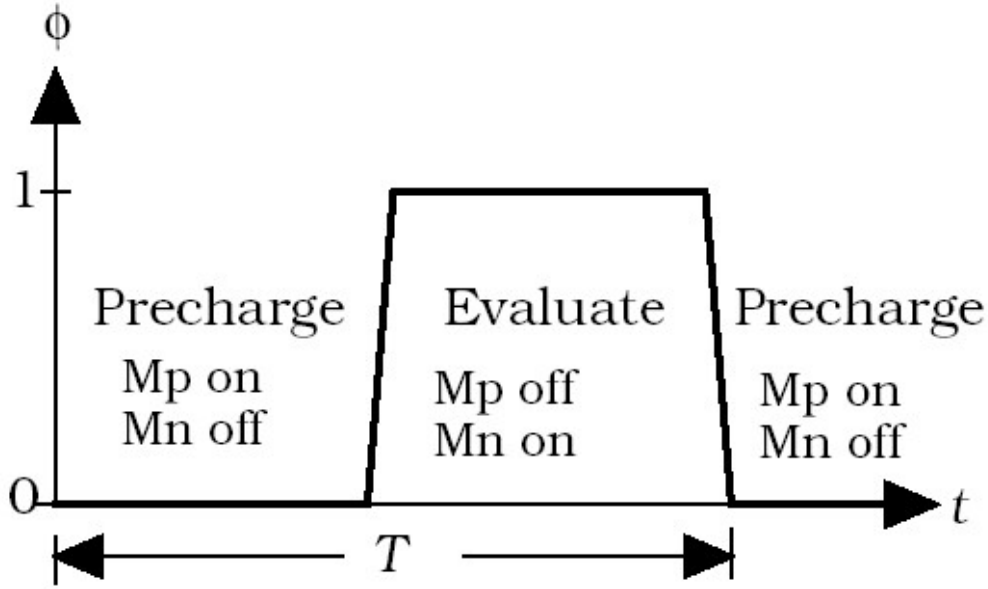


Figure 9.17 (p. 353)
Basic dynamic logic gate.

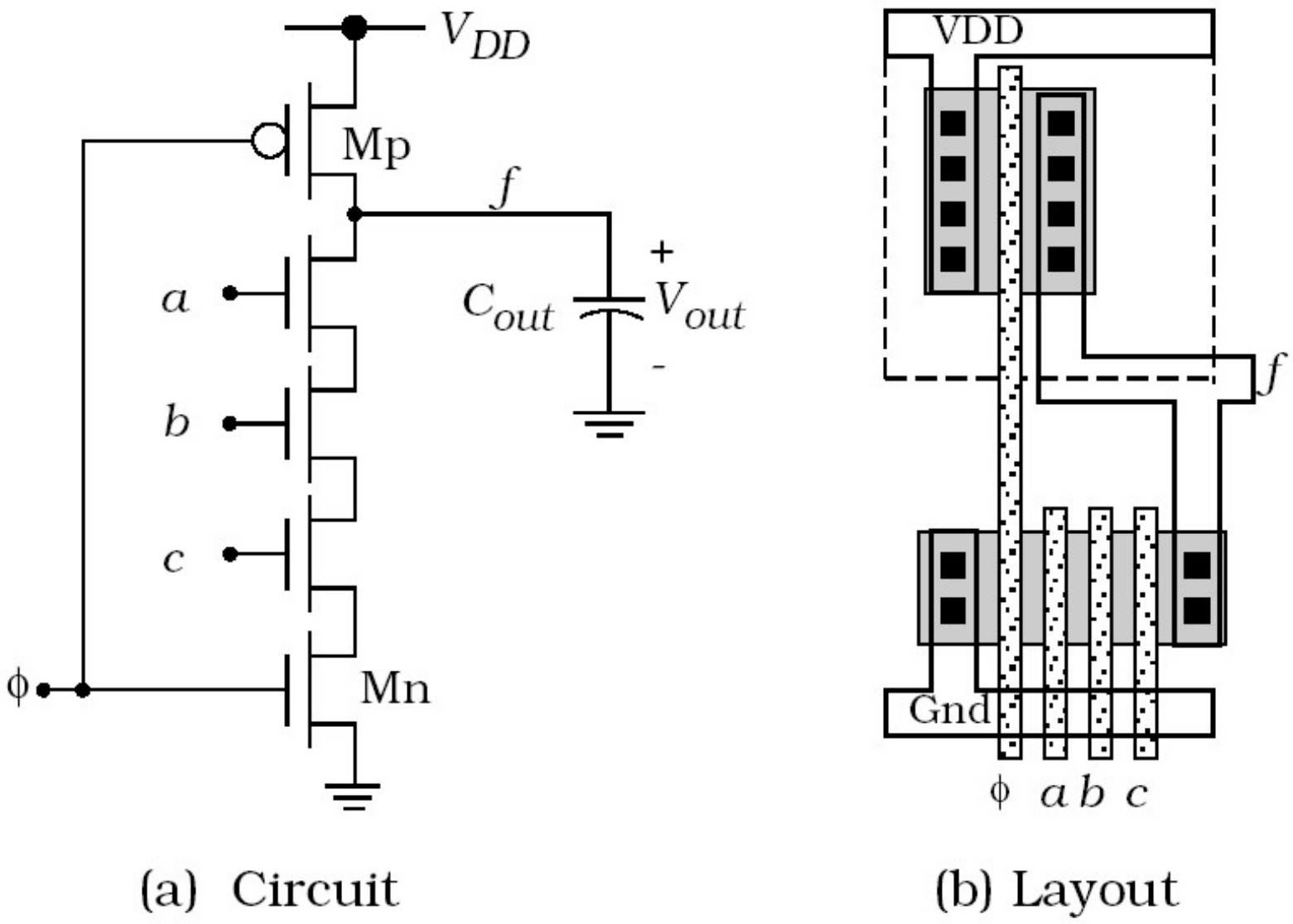


Figure 9.18 (p. 354)
Dynamic logic gate example.

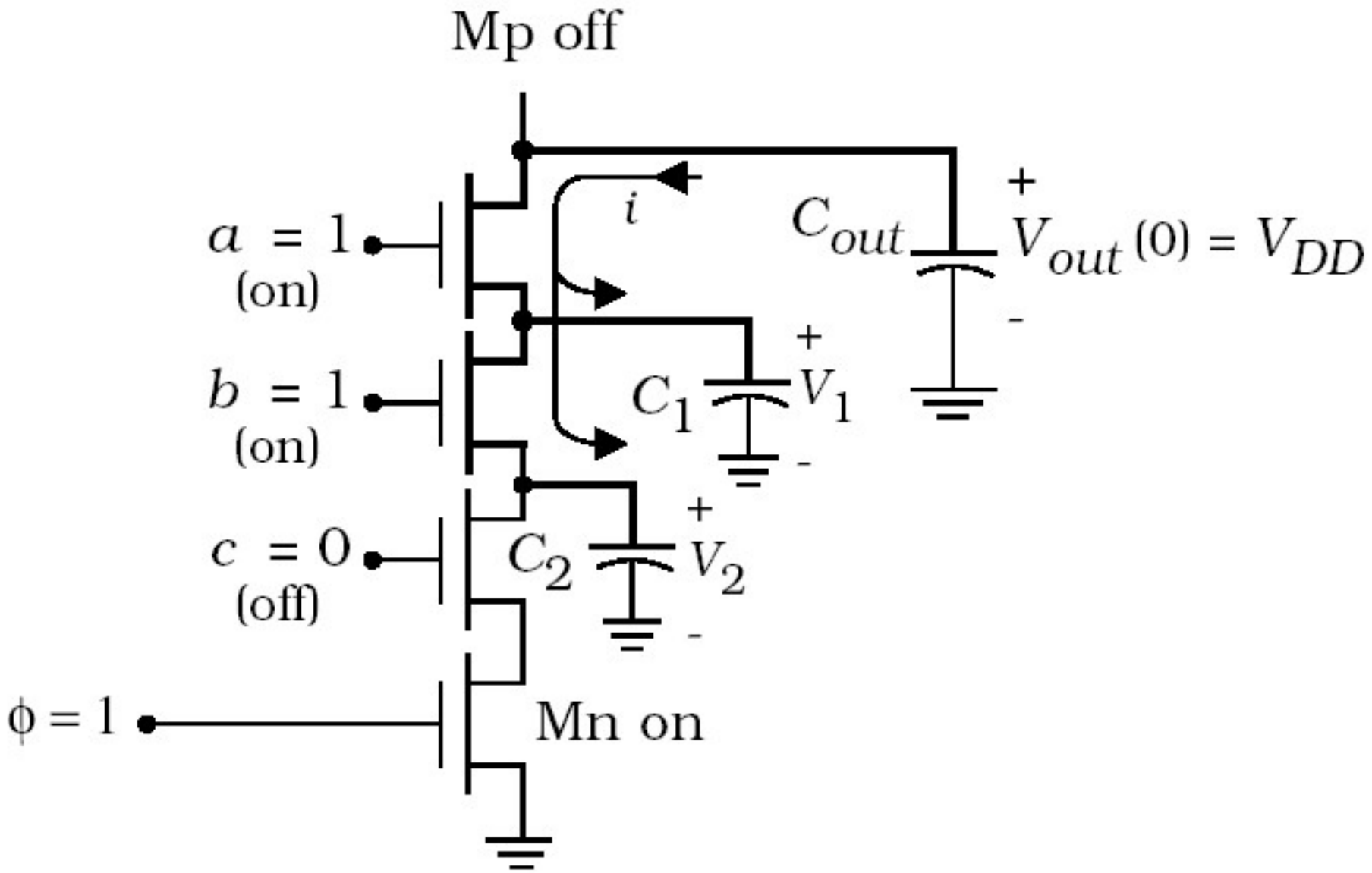


Figure 9.19 (p. 355)
Charge sharing circuit.

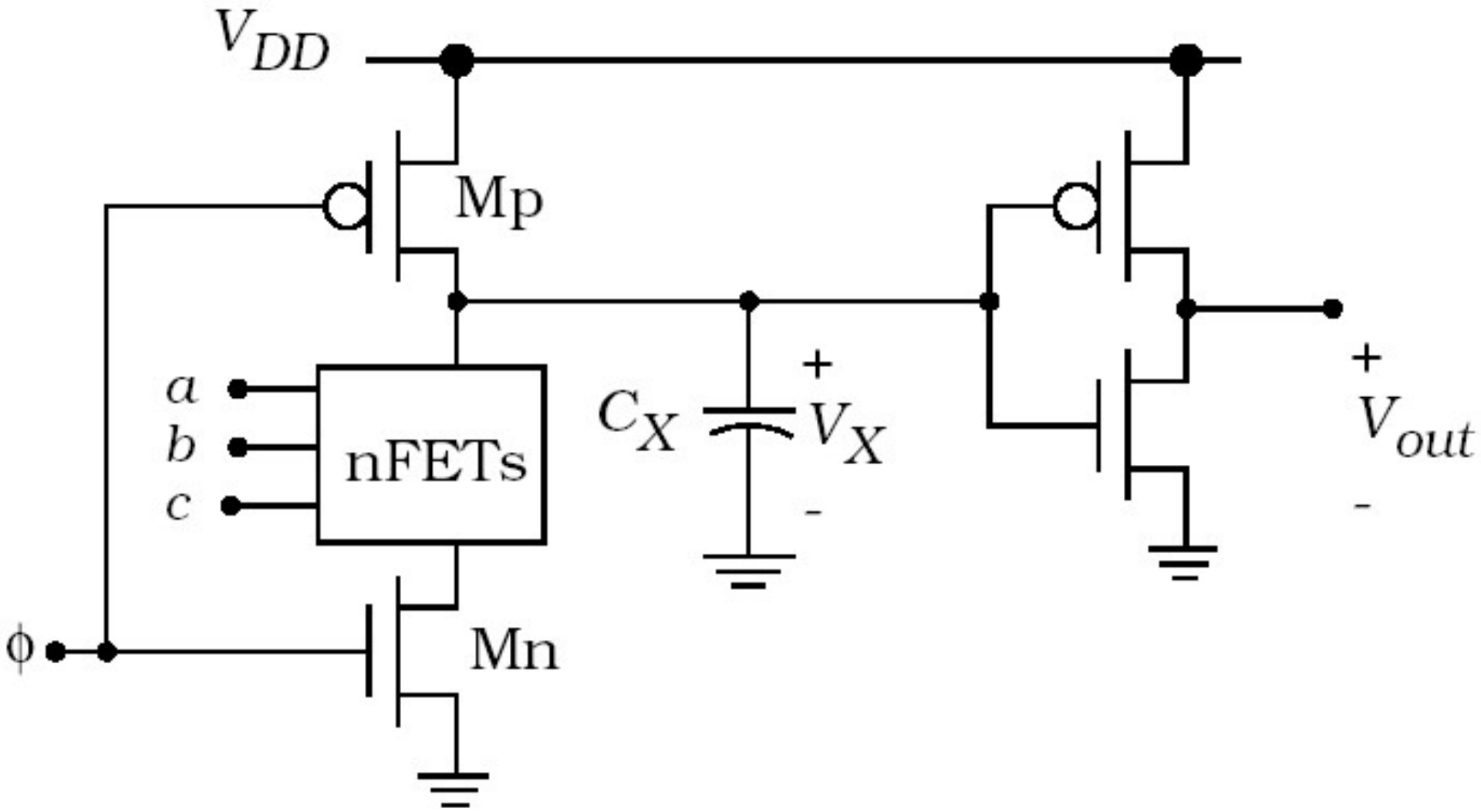


Figure 9.20 (p. 356)
Domino logic stage.

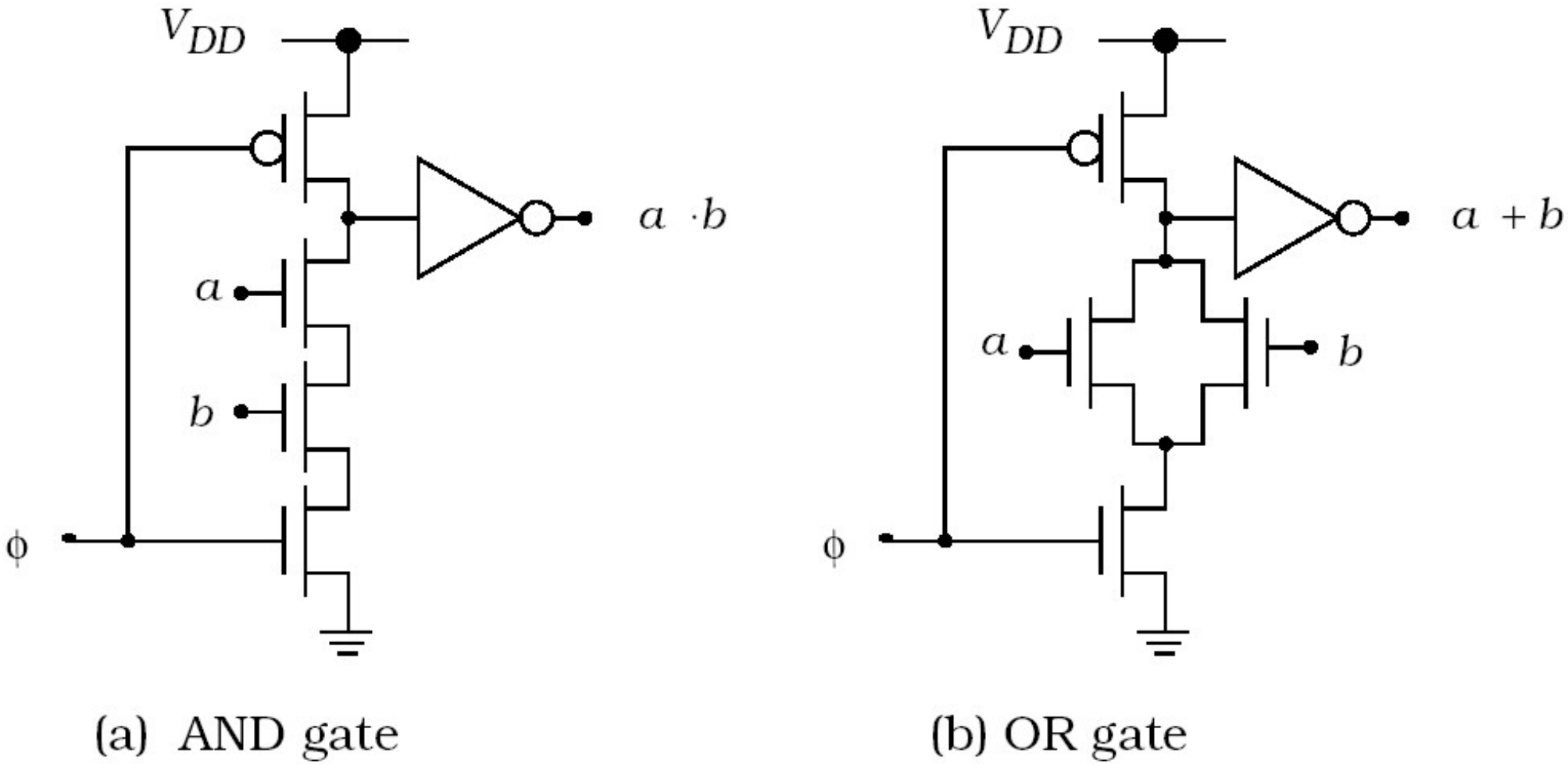


Figure 9.21 (p. 357)
Non-inverting domino logic gates.

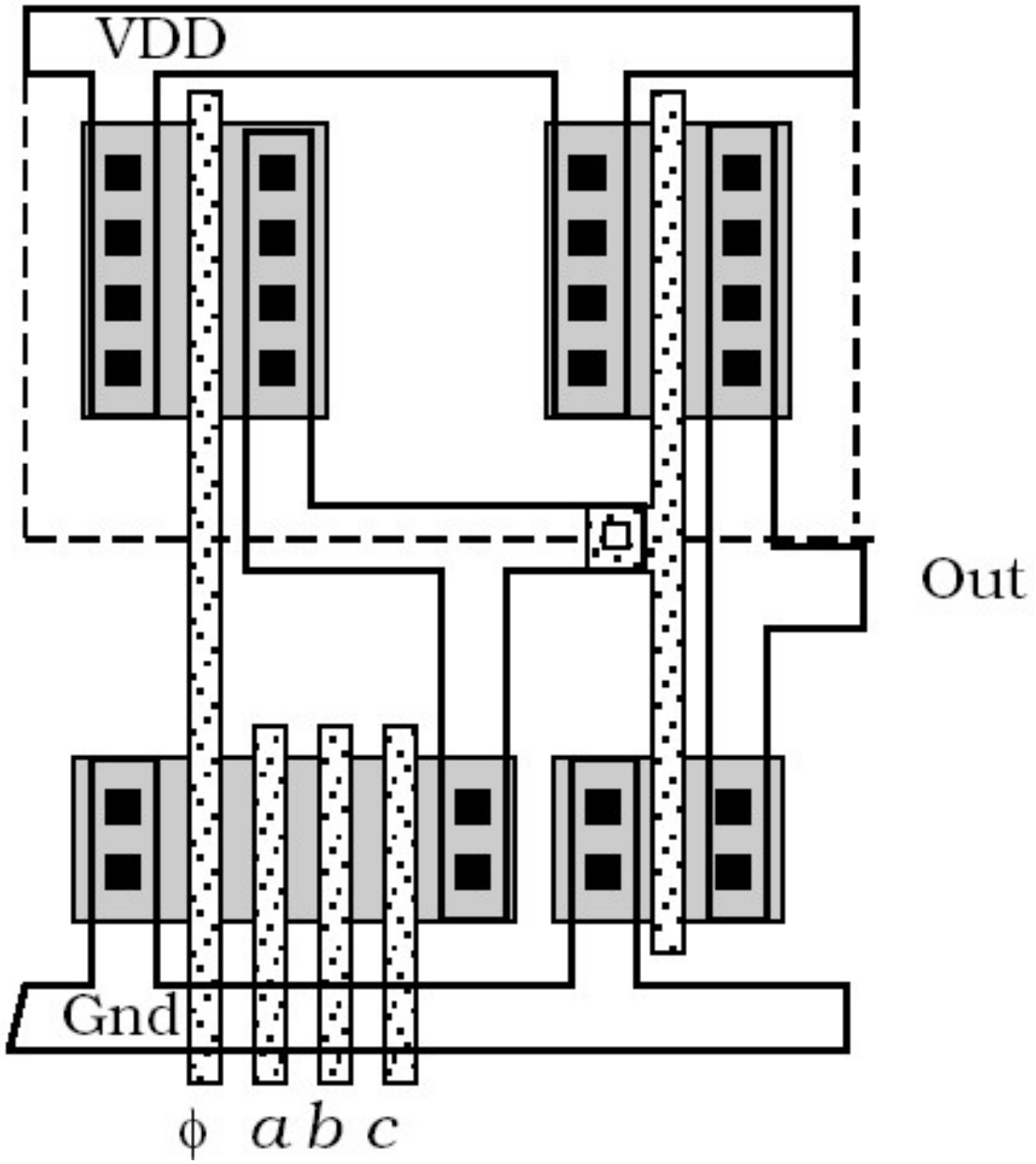


Figure 9.22 (p. 357)
Layout for a domino AND gate.

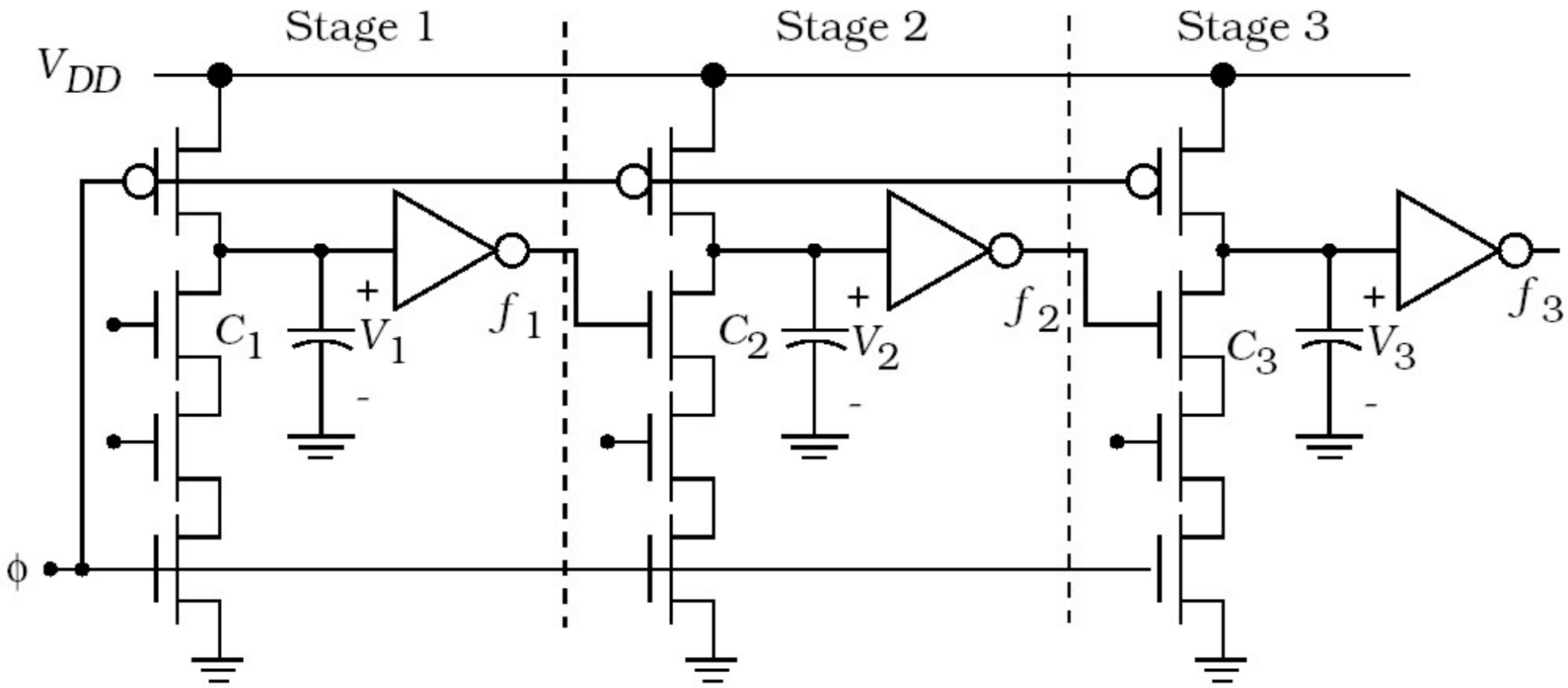


Figure 9.23 (p. 358)
A domino cascade.

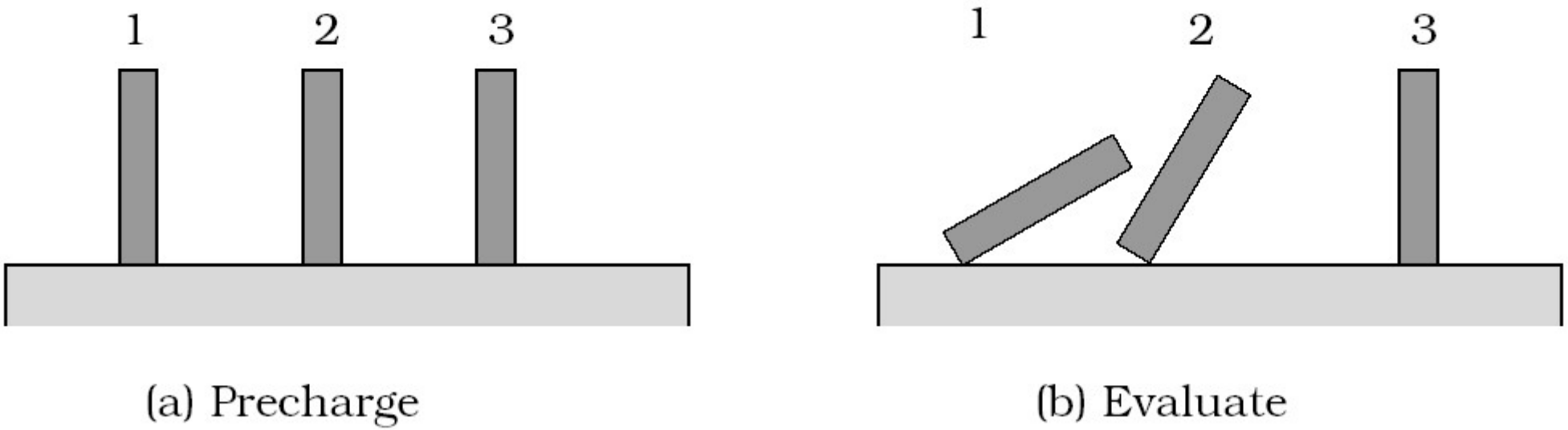
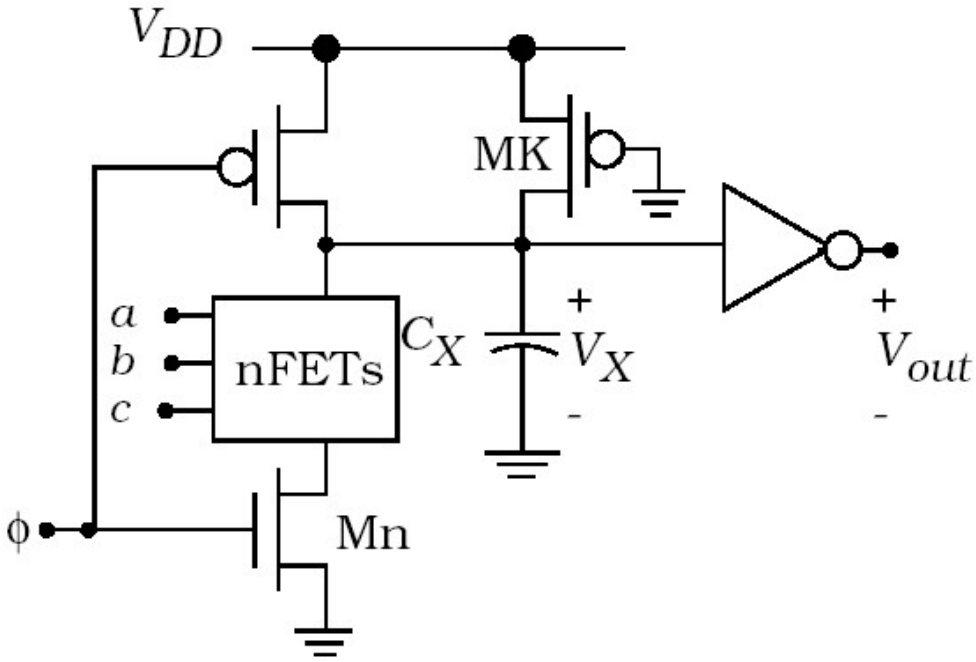
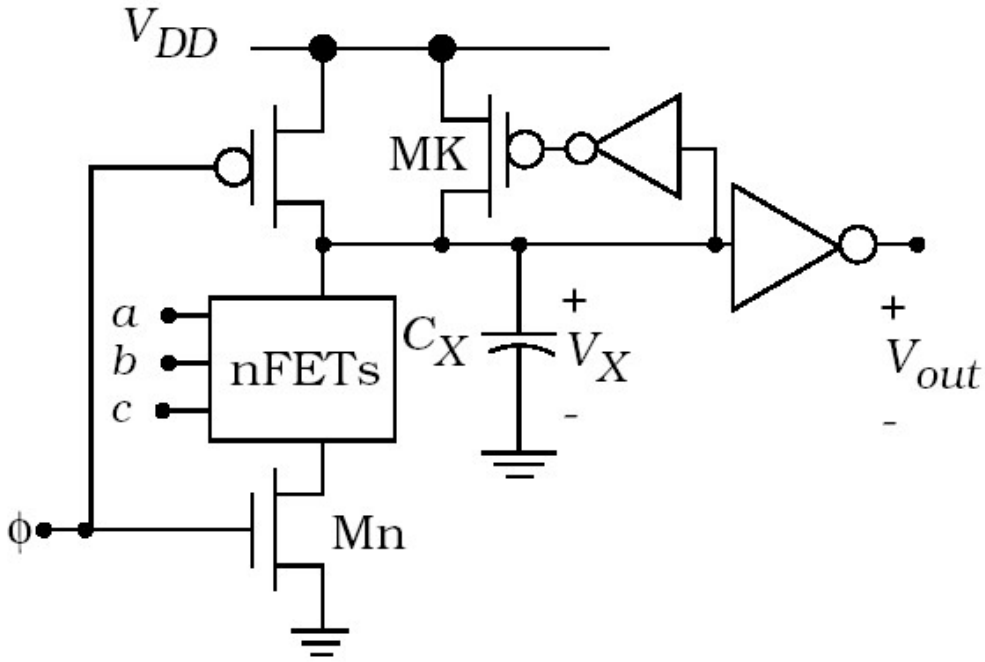


Figure 9.24 (p. 358)
Visualization of the domino effect.



(a) Single-FET charge keeper



(b) Feedback controlled keeper

Figure 9.25 (p. 359)
Charge-keeper circuits.

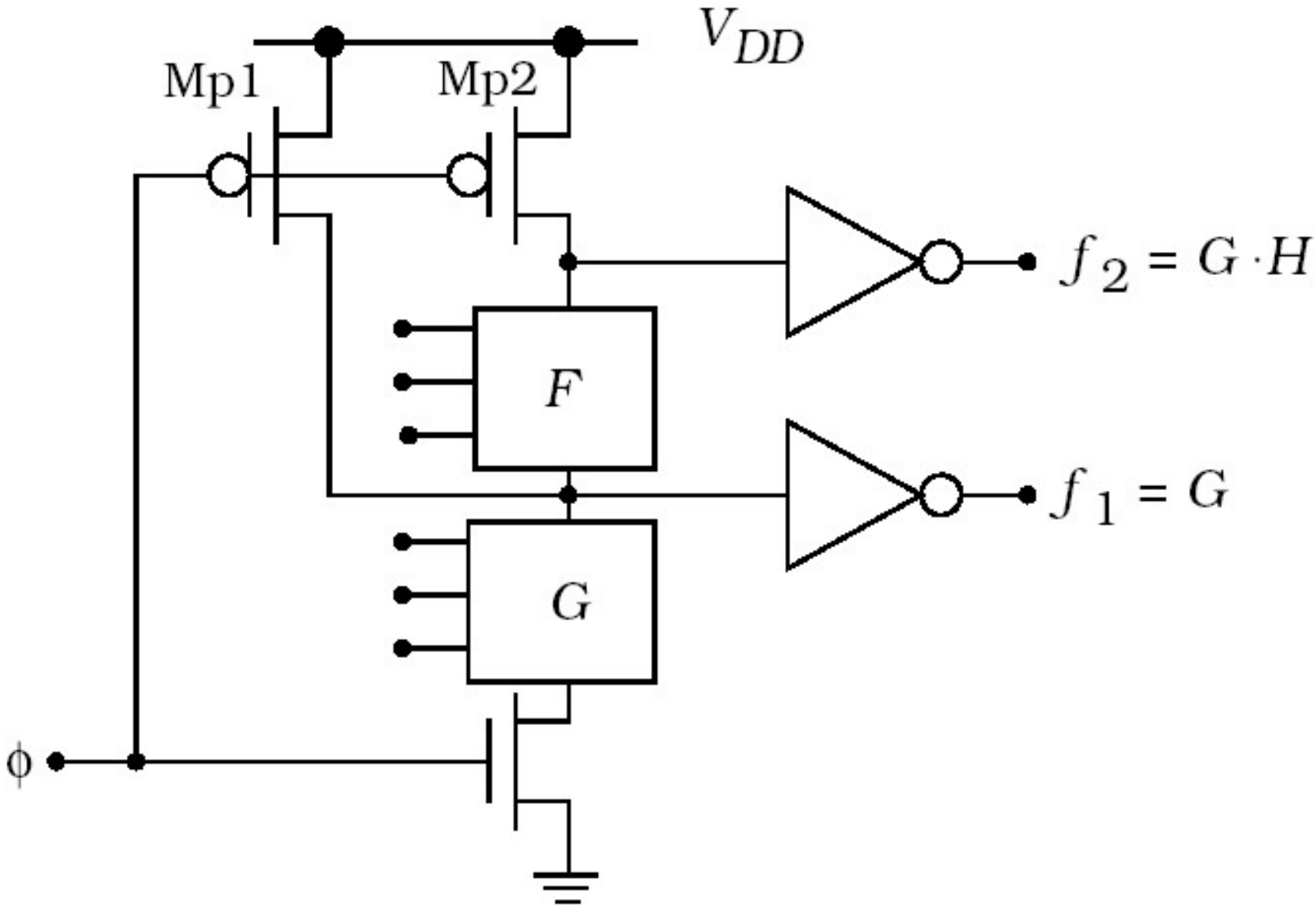


Figure 9.26 (p. 360)
Structure of a MODL circuit.

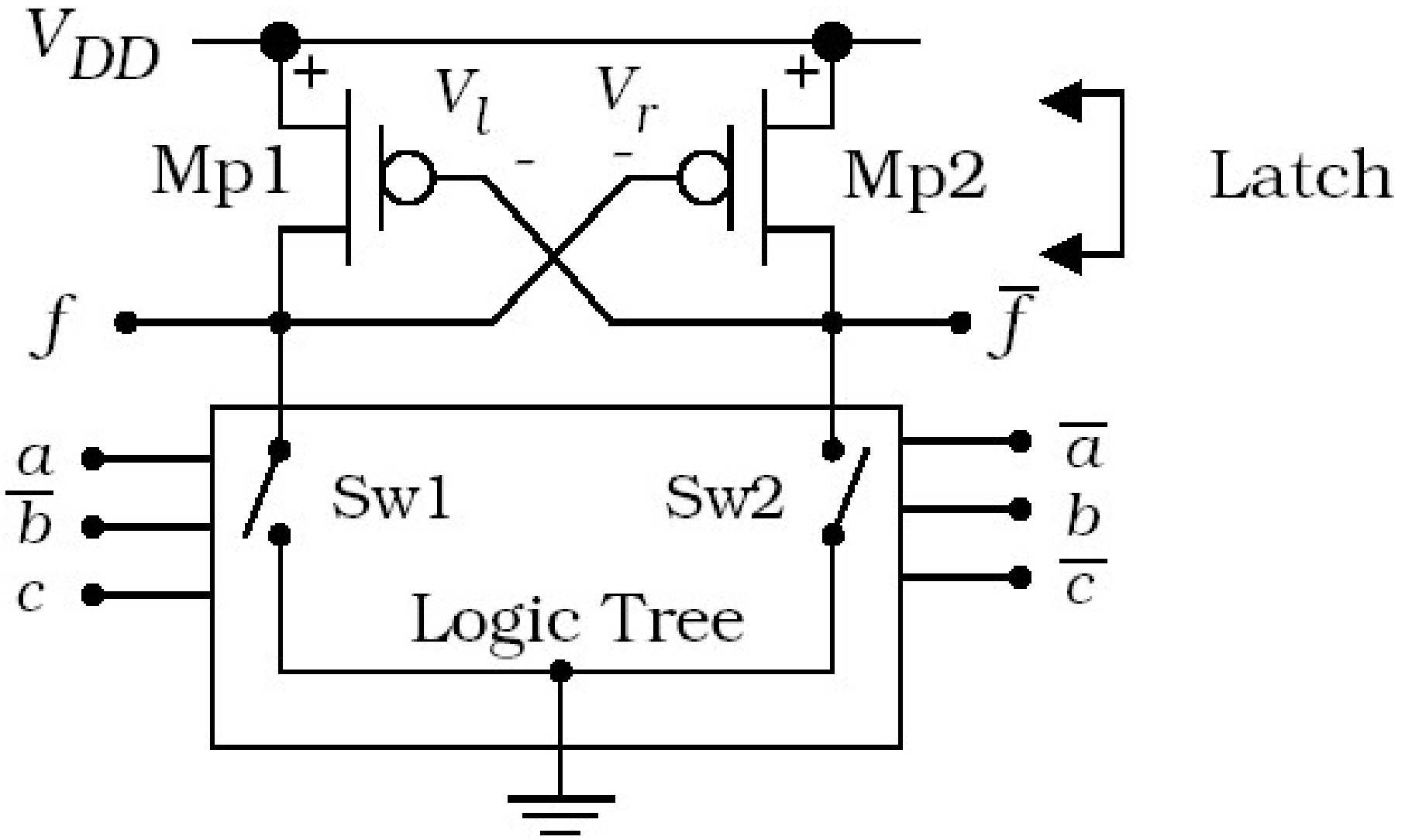
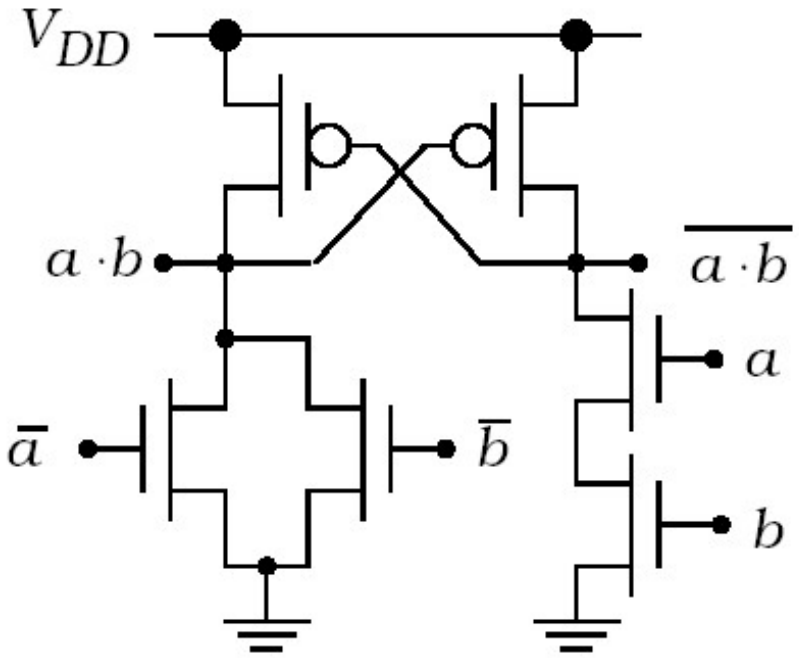
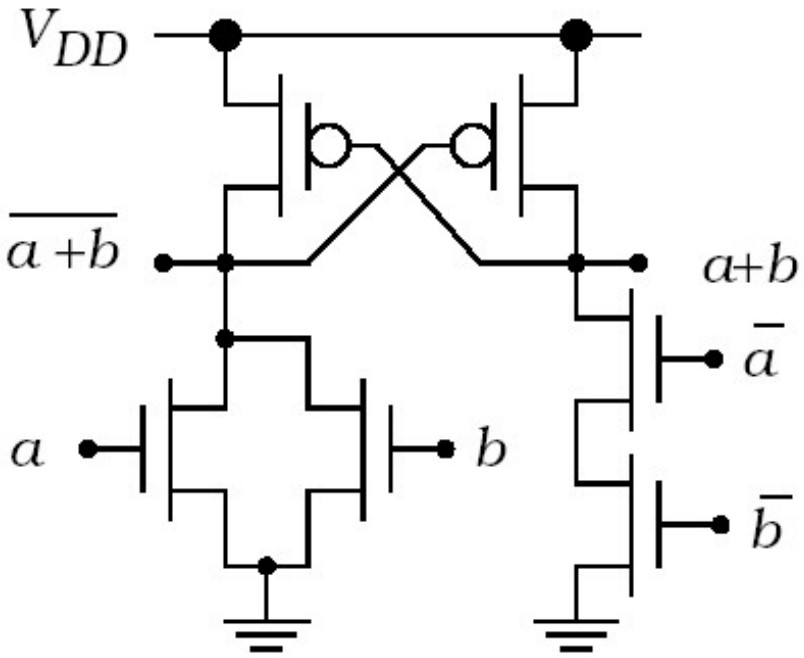


Figure 9.27 (p. 362)
Structure of a CVSL logic gate.

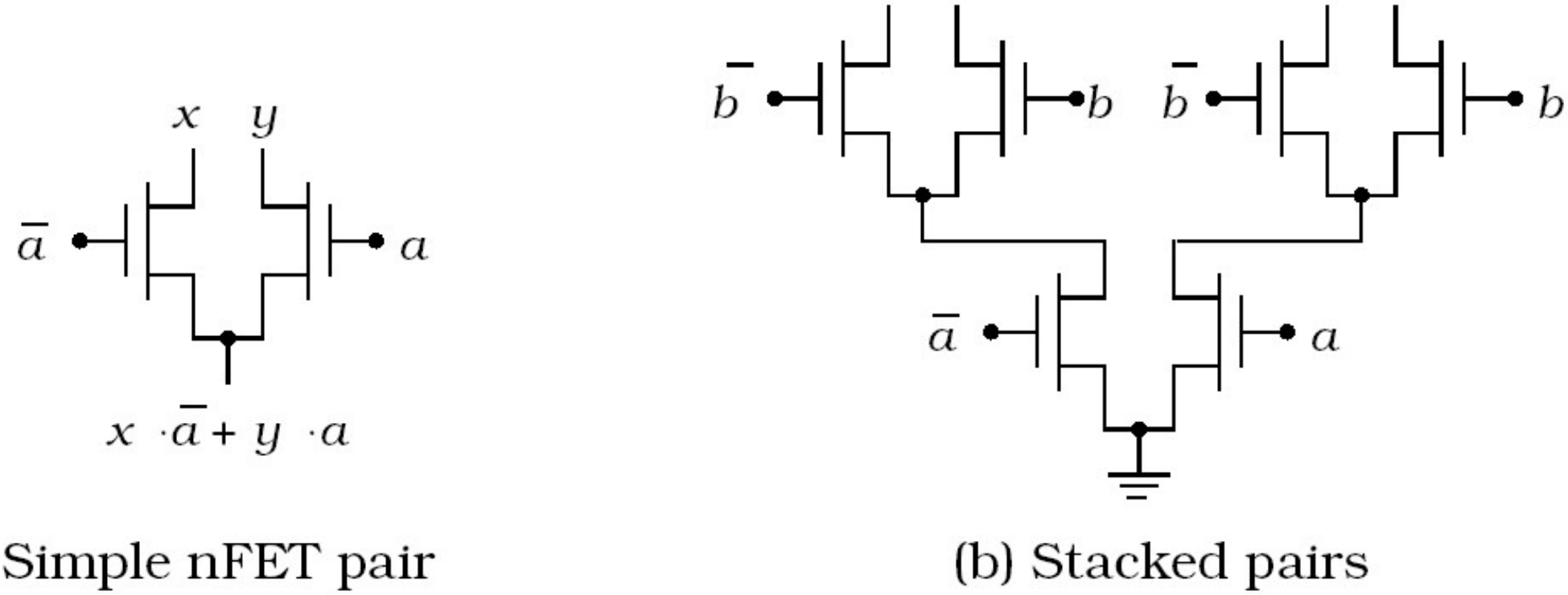


(a) AND/NAND



(b) OR/NOR

Figure 9.28 (p. 362)
CVSL gate examples.



(a) Simple nFET pair

(b) Stacked pairs

Figure 9.29 (p. 363)
nFET logic gates.

f	1	0	0	1
b	0	1	0	1
a	0	0	1	1

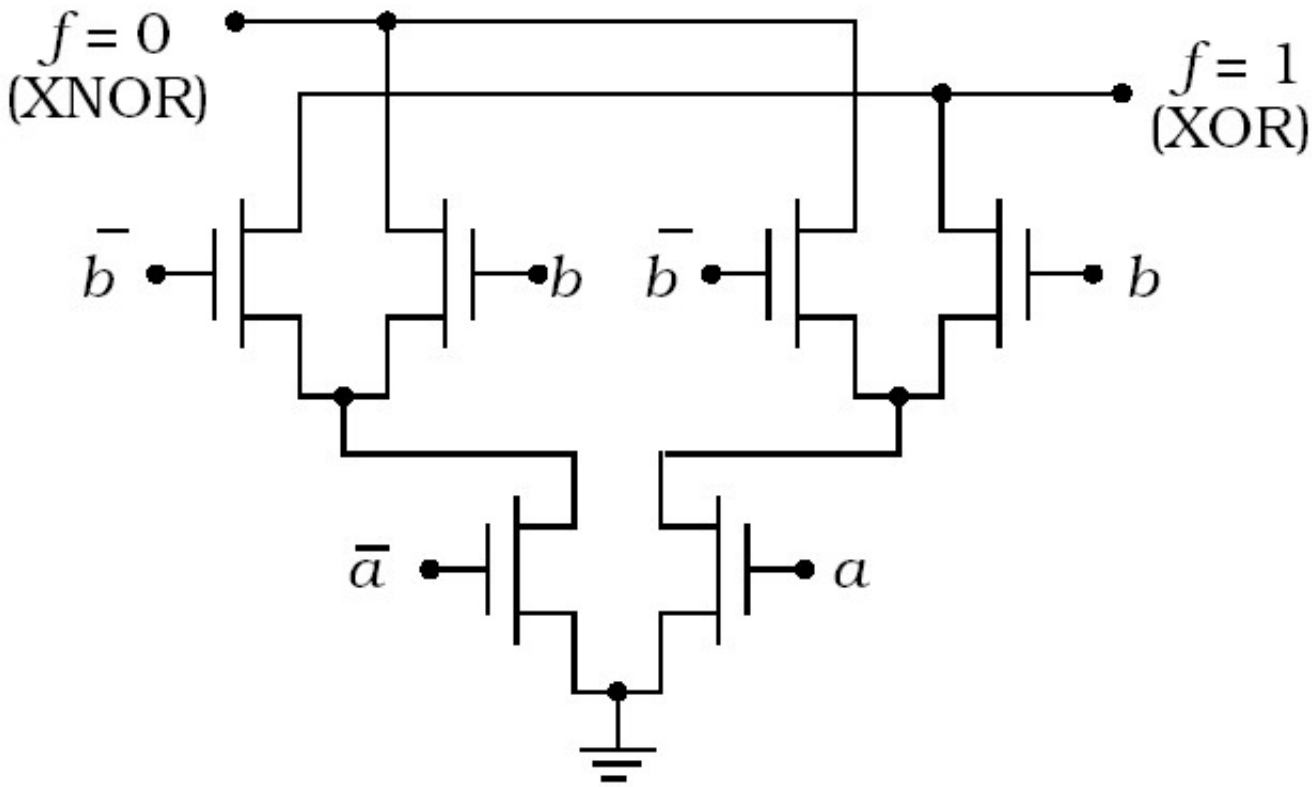
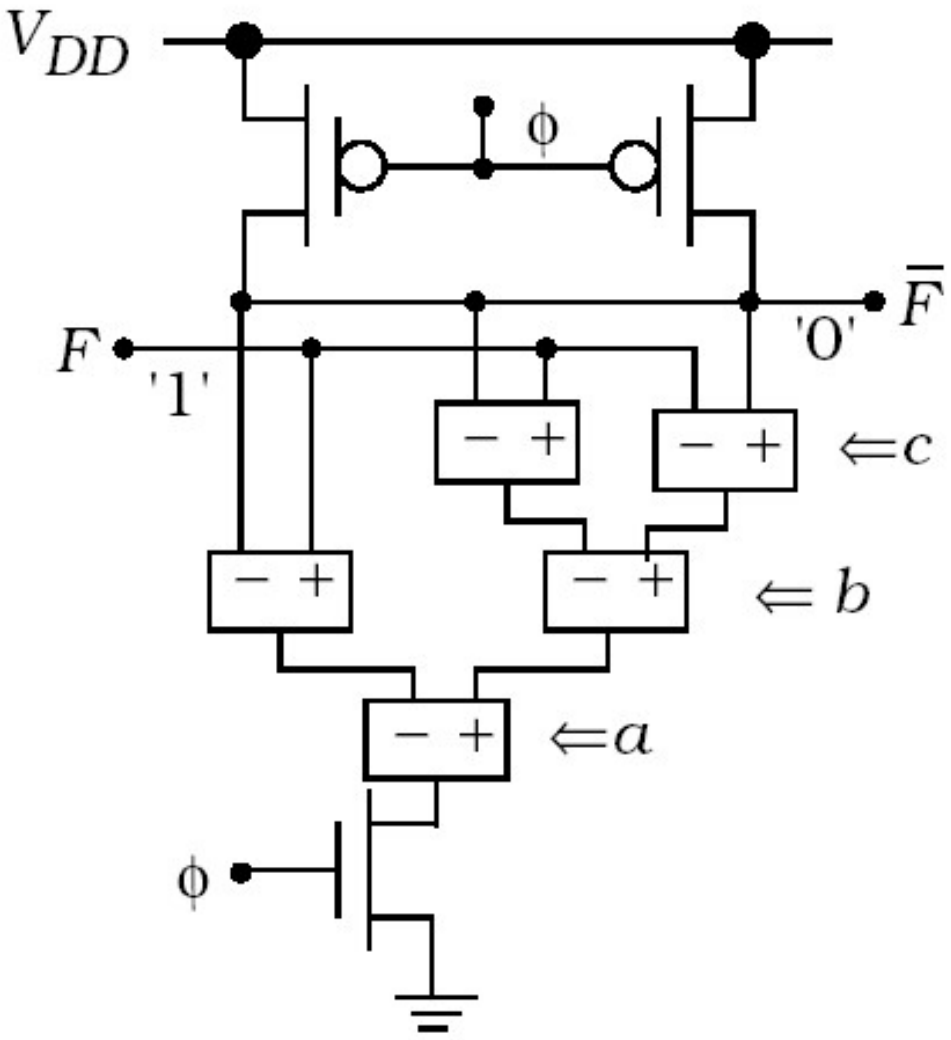


Figure 9.30 (p. 363)
Example of a logic tree using nFET pairs.



F	0	0	1	1	0	1	1	0
c	0	1	0	1	0	1	0	1
b	0	0	1	1	0	0	1	1
a	0	0	0	0	1	1	1	1

Figure 9.31 (p. 364)
Dynamic CVSL circuit with 3-level logic tree.