A More Precise Model of Noise Based PCMOS Errors

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Abstract. In this poster, we present a new model for characterization of probabilistic gates. While still not mainstream, probabilistic CMOS has the potential to dramatically reduce energy consumption by trading off with error rates on individual bits, e.g., least significant bits of an adder. Our contribution helps account for the filtering effect seen in noise based PCMOS in a novel way. The characterization proposed here can enable accurate multi-bit models based on fast mathematical extrapolation instead of expensive and slow HSPICE simulations.

II. Previous probabilistic ripple-carry adder (PRCA) model [2] is inaccurate, as shown by HSPICE simulation.

III. Why is it inaccurate?

IV. A more accurate PRCA model capturing noise filtering effect.

V. References