NANYANG TECHNOLOGICAL UNIVERSITY

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A More Precise Model of Noise Based PCMOS Errors

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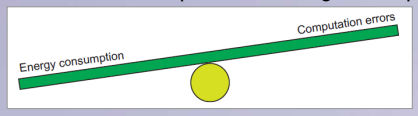
Abstract. In this poster, we present a new model for characterization of probabilistic gates. While still not mainstream, probabilistic CMOS has the potential to dramatically reduce energy consumption by trading off with error rates on individual bits, e.g., least significant bits of an adder. Our contribution helps account for the filtering effect seen in noise based PCMOS in a novel way. The characterization proposed here can enable accurate multi-bit models based on fast mathematical extrapolation instead of expensive and slow HSPICE simulations.

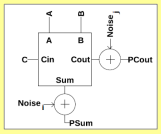
I. What is probabilistic computing?

- Technology that allows computation with occasional erroneous arithmetic operations [1].
- Trading correctness of circuit operations for significant power saving.



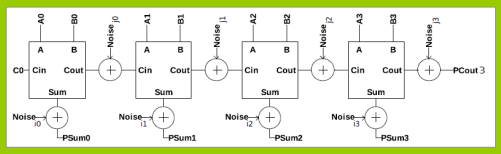
II. Previous probabilistic ripple-carry adder (PRCA) model [2] is inaccurate, as shown by HSPICE simulation.

HSPICE simulation of a probabilistic full-adder (PFA)

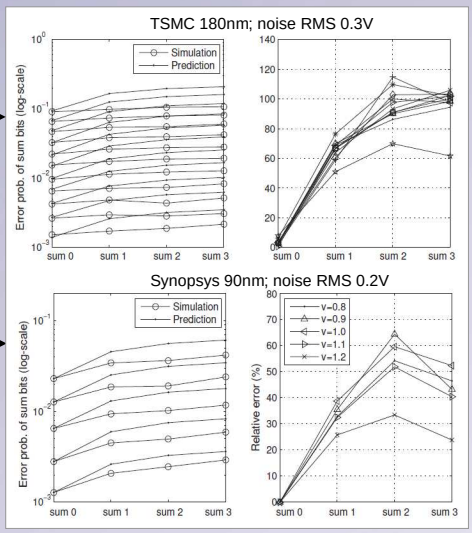


→ Carry-out and sum error-rates of a PFA → Closed-form mathematical formula [3] → Predicted sum error-rates of a multi-bit PRCA

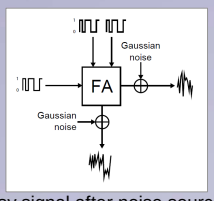
HSPICE simulation of a multi-bit PRCA



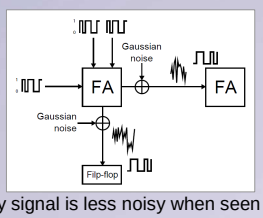
→ Sum error-rates of the simulated multi-bit PRCA



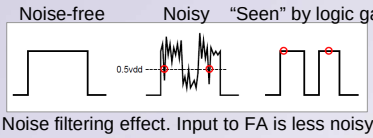
III. Why is it inaccurate?



Noisy signal after noise source



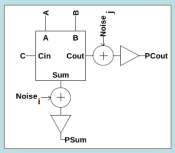
The same noisy signal is less noisy when seen by a logic gate.



Noise filtering effect. Input to FA is less noisy

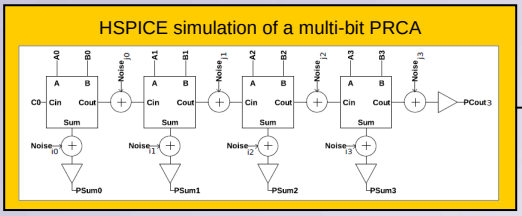
IV. A more accurate PRCA model capturing noise filtering effect.

HSPICE simulation of a PFA

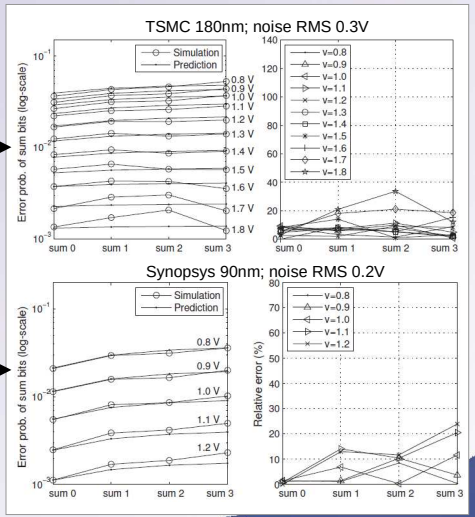


→ Carry-out and sum error-rates of a PFA → Closed-form mathematical formula [3] → Predicted sum error-rates of a multi-bit PRCA

HSPICE simulation of a multi-bit PRCA



→ Sum error-rates of the simulated multi-bit PRCA



V. References

[1] Palem, "Energy aware computing through probabilistic switching: a study of limits," IEEE Transactions on Computers, vol. 54, no. 9, pp. 1123-1137, 2005.
[2] George et al., "Probabilistic arithmetic and energy efficient embedded signal processing," Proceedings of CASES 2006, pp. 158-168, 2006.
[3] Lau et al., "Modeling of probabilistic ripple-carry adders," Proceedings of DELTA 2010.