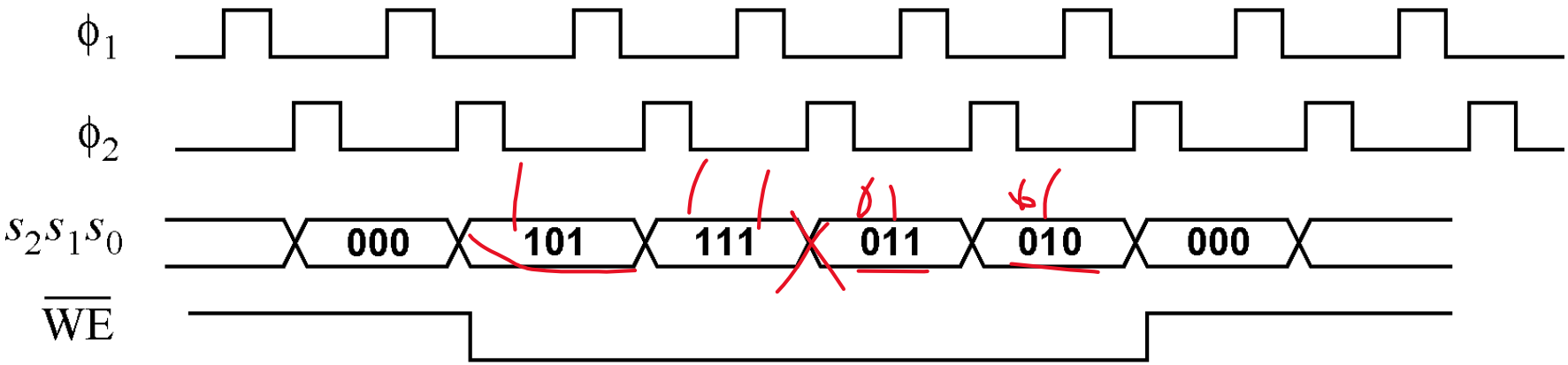
# ECE 3060
# VLSI and Advanced Digital Design

## Hazards

# Motivation

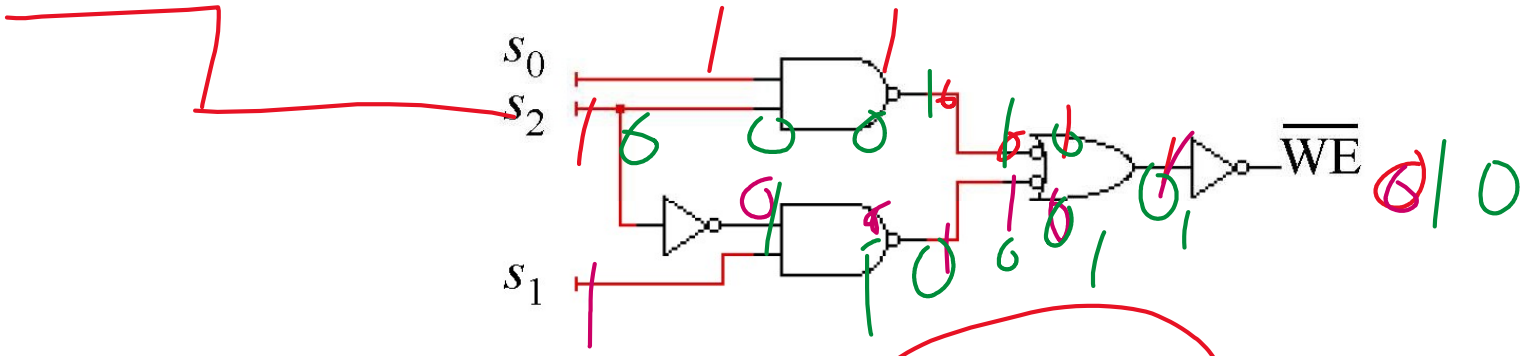
**Suppose we wish a logic signal (say a DRAM $\overline{\text{WE}}$ signal) to be glitch free**

**Suppose the signal is generated by four states of a state machine as shown**




**Minimization yields** $\overline{\text{WE}} = \overline{(s_2 s_0 + \overline{s_2} s_1)}$

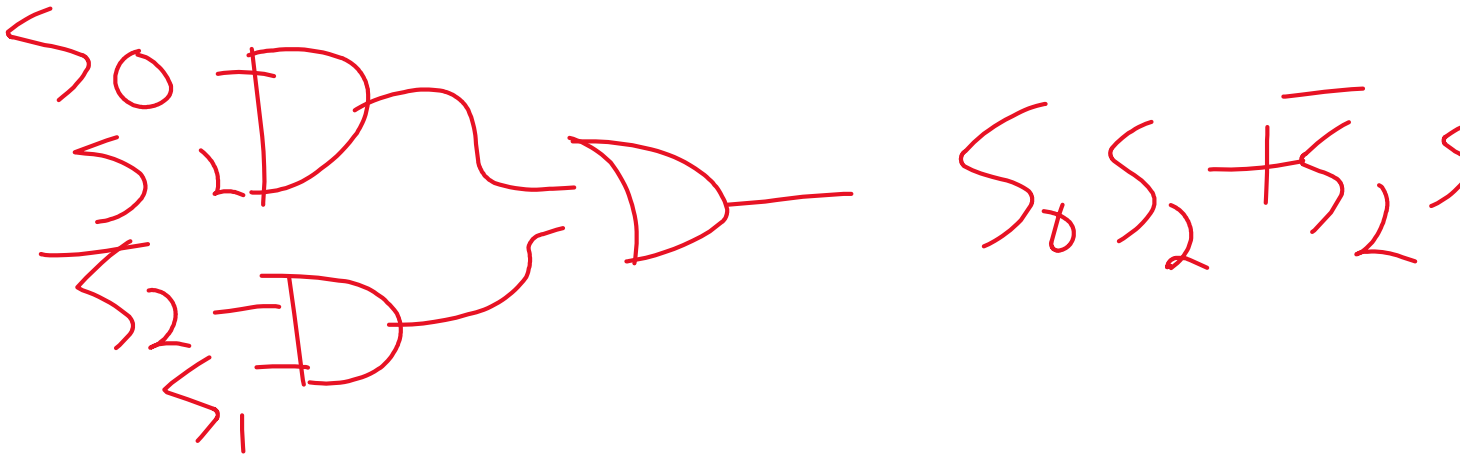
# Implementation

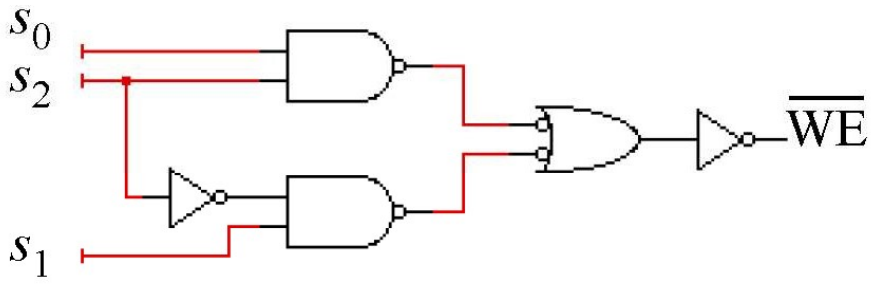



**Consider transition $S = 111$ to $S = 011$**

**This cause of this glitch is a static 1 hazard in the implementation.**

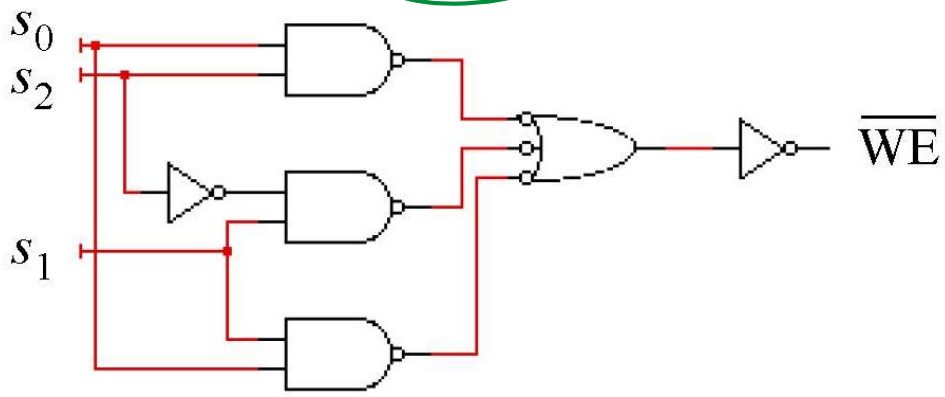
**A static 1 hazard is present whenever adjacent 1 nodes on the cube are not covered by the same implicant**




$s_0$
$s_2$
$s_1$
$\overline{\text{WE}}$

# Solution

**Add the consensus term $s_1 s_0$**




**An analogous case exists for a static 0 hazard in a product of sums expression**

**Dynamic hazards are much more difficult to analyze, and occur in multi-level logic and where multiple inputs may change concurrently.**