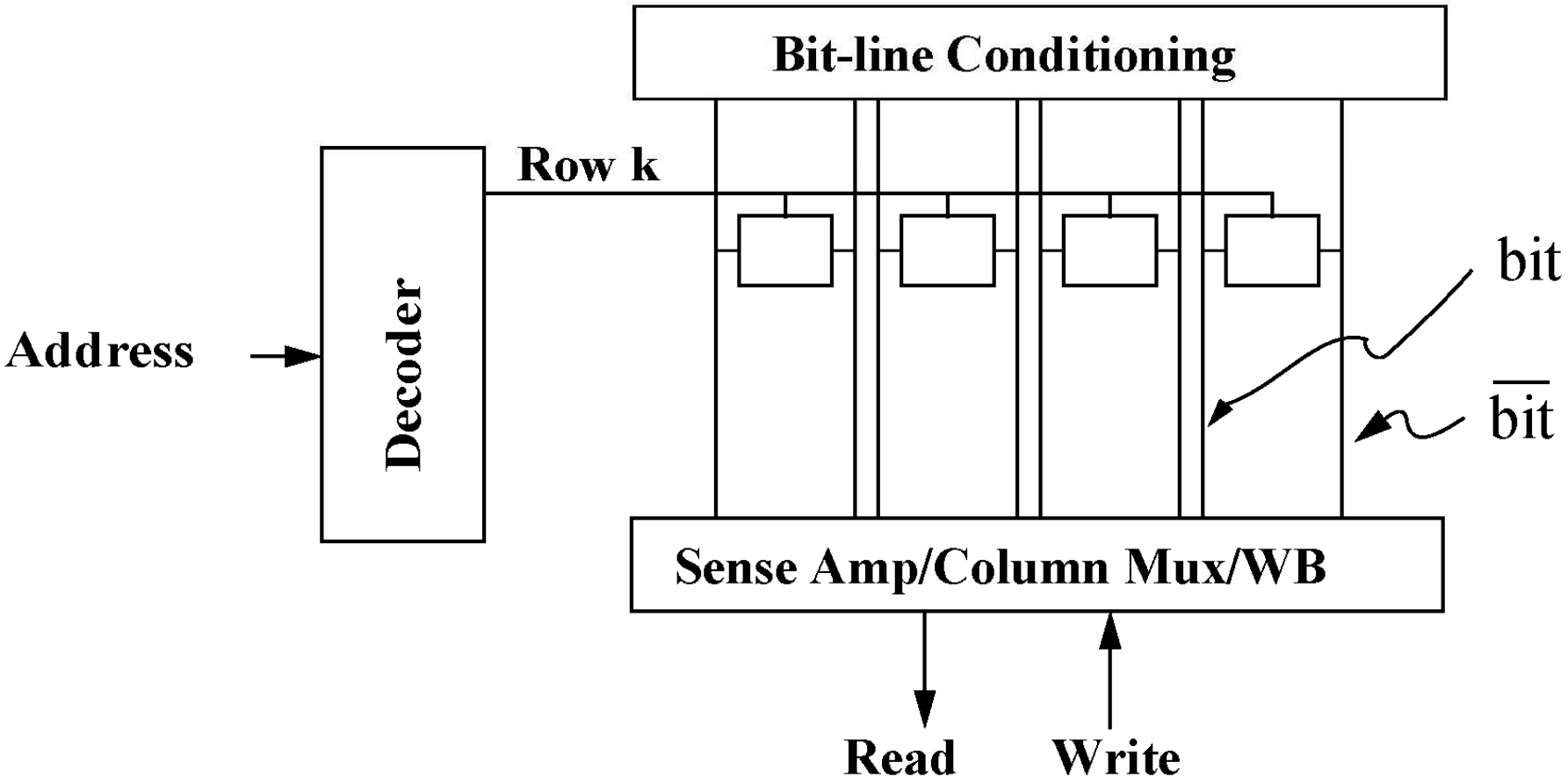
ECE 6130
VLSI and Advanced Digital Design

Memory

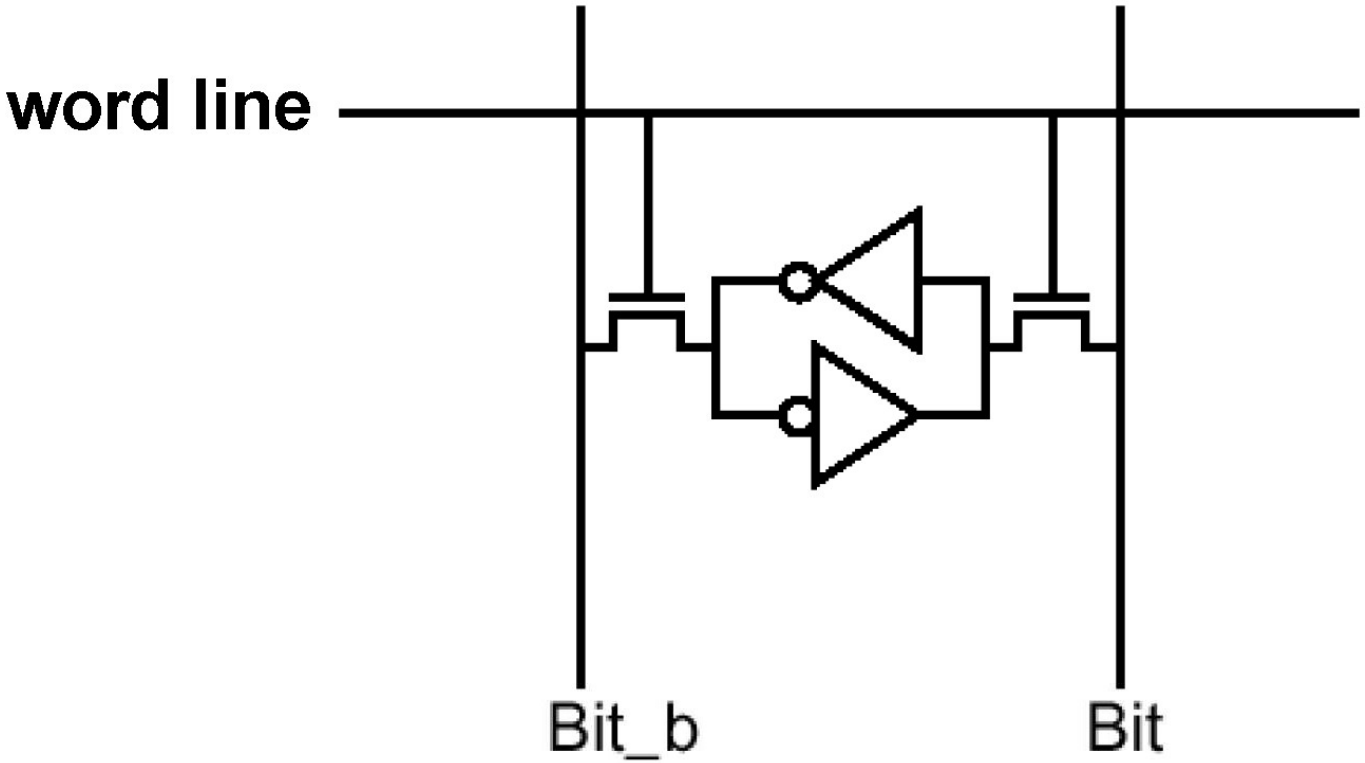
RAM Organization



- Data is carried on complementary bit busses
- Cell design must consider analog behavior

SRAM Cell

- SRAM cell is designed for density, power, and speed
- Basic cell uses 6T



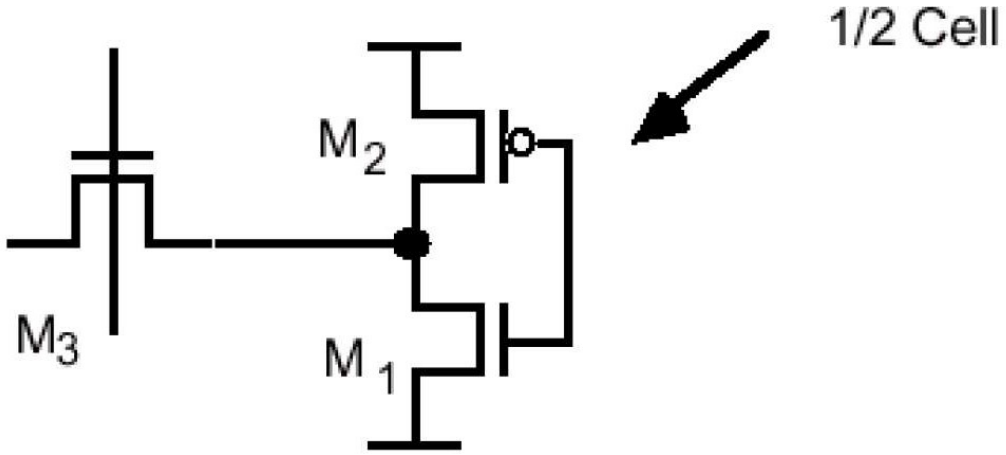
- SRAM transistor βs are critical

SRAM Operation

- The key issue in an 6T SRAM is how to distinguish between read and writes.
- There is only one wordline, so it must be high for both reads and writes. The key is to use the fact there are two bitlines.
- Read: Both Bit and Bit_b must start high. A high value on the bitline does not change the value in the cell, so the cell will pulls one of the lines low
- Write:
  - One (Bit or Bit_b) is forced low, the other is high
  - This low value overpowers the pMOS in the inverter, and this will write the cell.

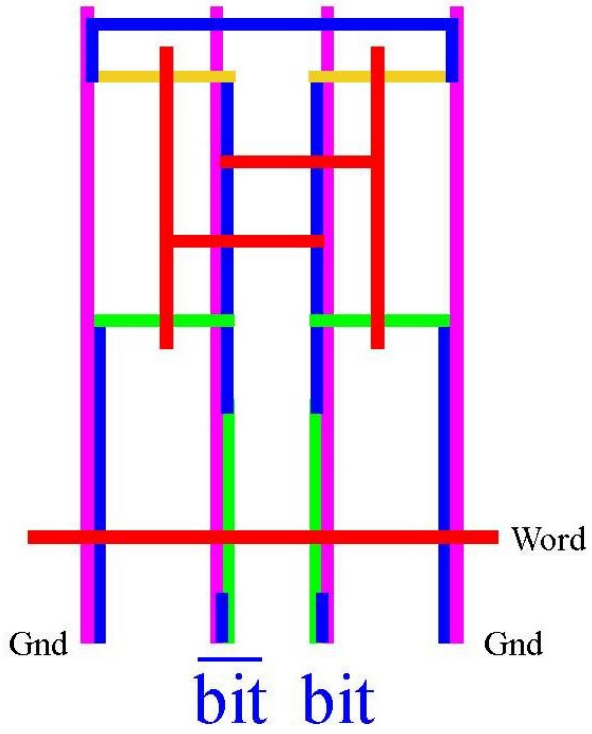
Transistor Sizing

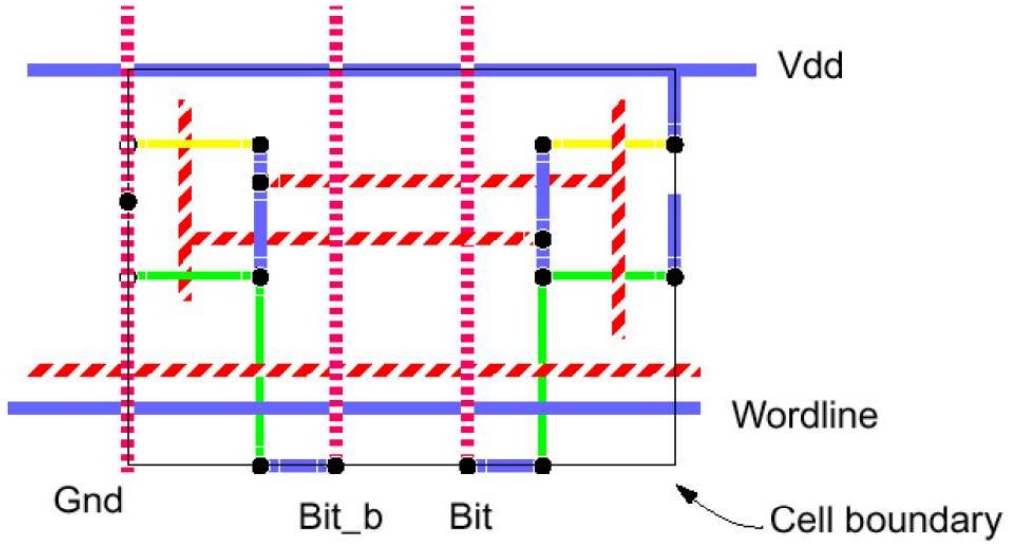
- For the cell to work correctly a zero on the bit line must over power the pMOS pullup, but a one on the bit line must not over power the pull down (otherwise reads would not work)



- For the pull down M3 is passing a zero, so for it to overpower the pMOS it must be at least as wide (preferably 1.5x as wide). This gives a 2-3:1 current ratio between the nMOS and the pMOS.
- For pull up M3 is passing a one so it is somewhat weaker. Still M3 should be 1.5 to 2x smaller than M1 to make sure a read does not disturb the value of the cell.

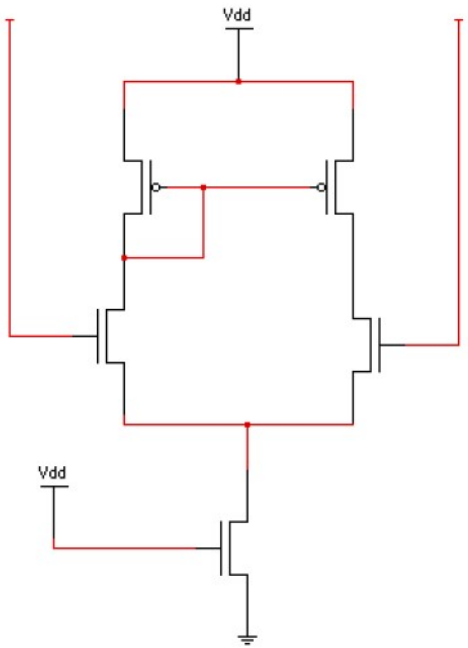
Common Layout





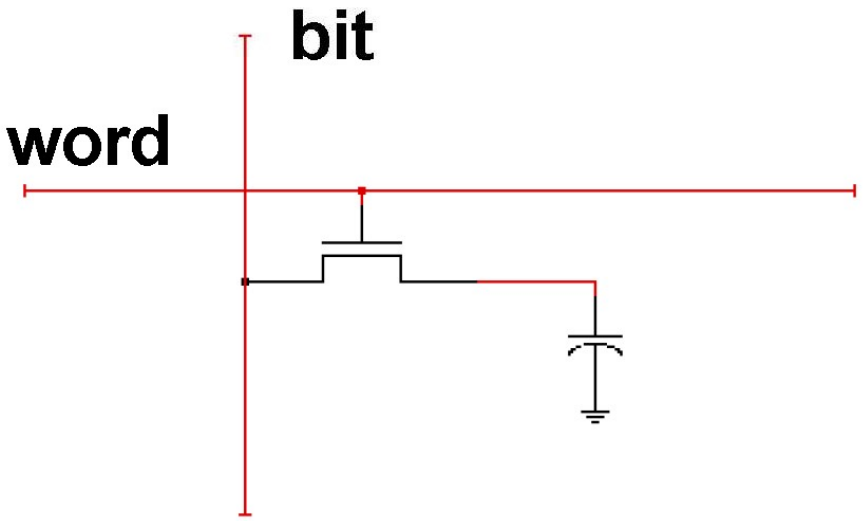
SRAM Read

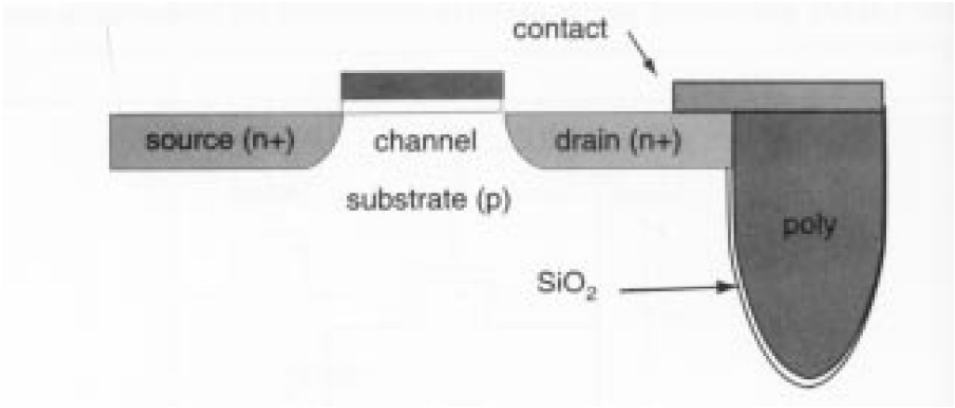
- **Read operation is performed by sense amplifier. As** Bit **and** $\overline{\text{Bit}}$ **diverge, the sense amp will detect the divergence and amplify the difference.**
- **Sense amp is usually implemented with a differential amplifier.**



DRAM

- Basic DRAM is 1T design:





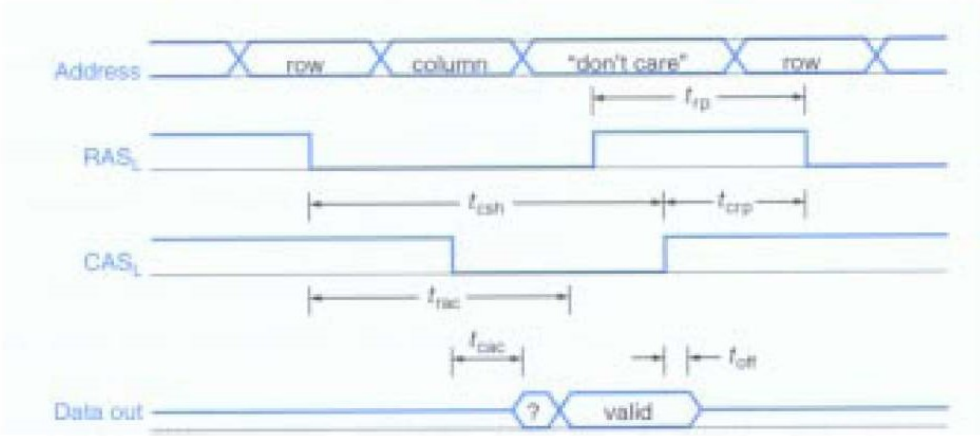
- Capacitor is special vertical trench design

DRAM Quirks

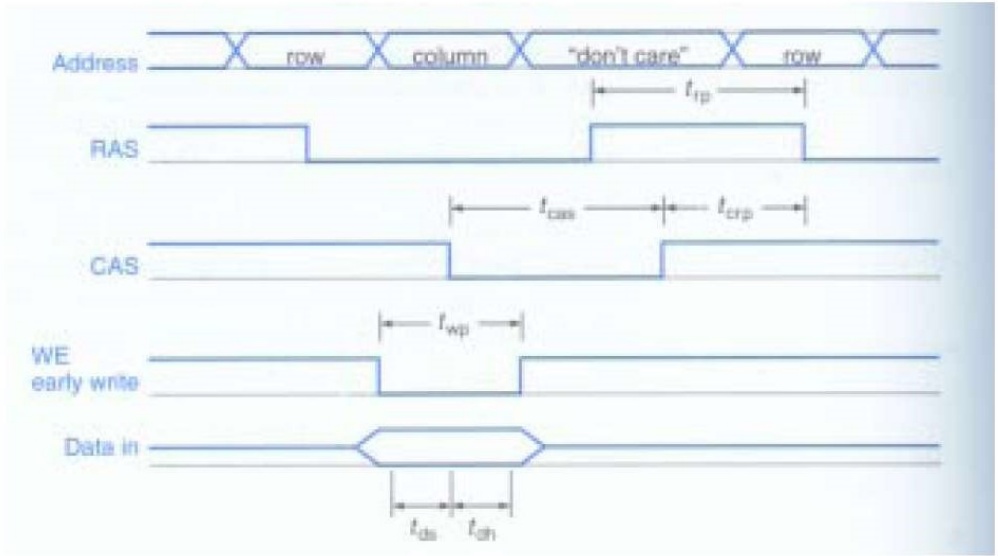
- Leakage current means stored value will decay over time (stable for several ms)
  - neccessity for refresh
- Read is destructive
  - Data must be written back to a row of DRAM after it is read
- Because of the very fine horizontal pitch of a DRAM cell (few lambda), a DRAM row is many times wider than the output row of the array.
  - The column address selects which column of the array will be accessed
- Historical pin limitations
  - row and column addresses multiplexed on address bus and latched by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals

Typical DRAM Timing

- **Read timing**



- **Write timing**



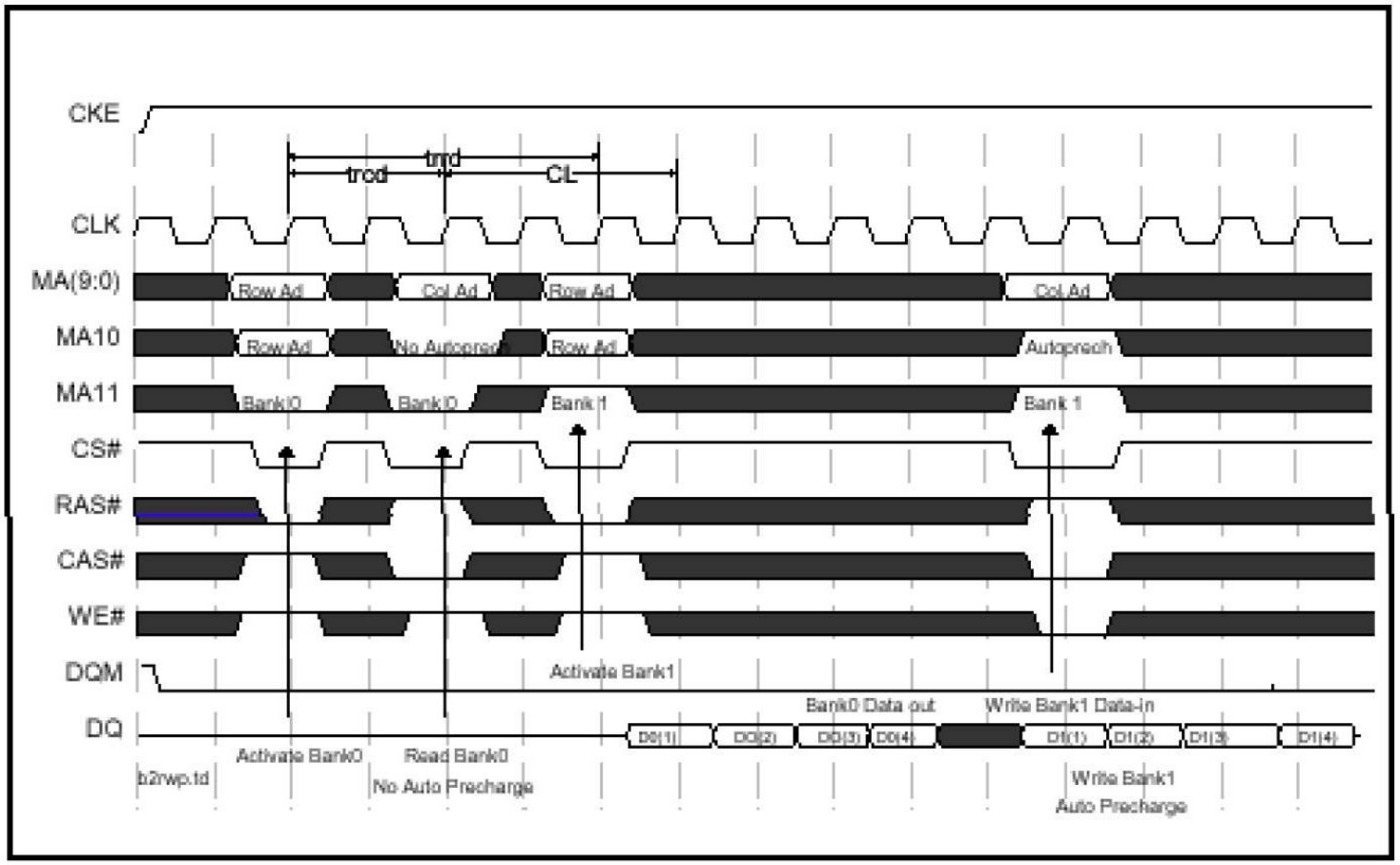
Details

- Write is really
  - read row into row buffer
  - modify word selected by column address
  - write modified row back
- Refresh cycle is read-nomodify-writeback
- Throughput and access latency is limited by combinational delays through row decoders, access of row, and column select
- Burst mode: for a given row address, sequence through successive column addresses accessing data already in row buffer

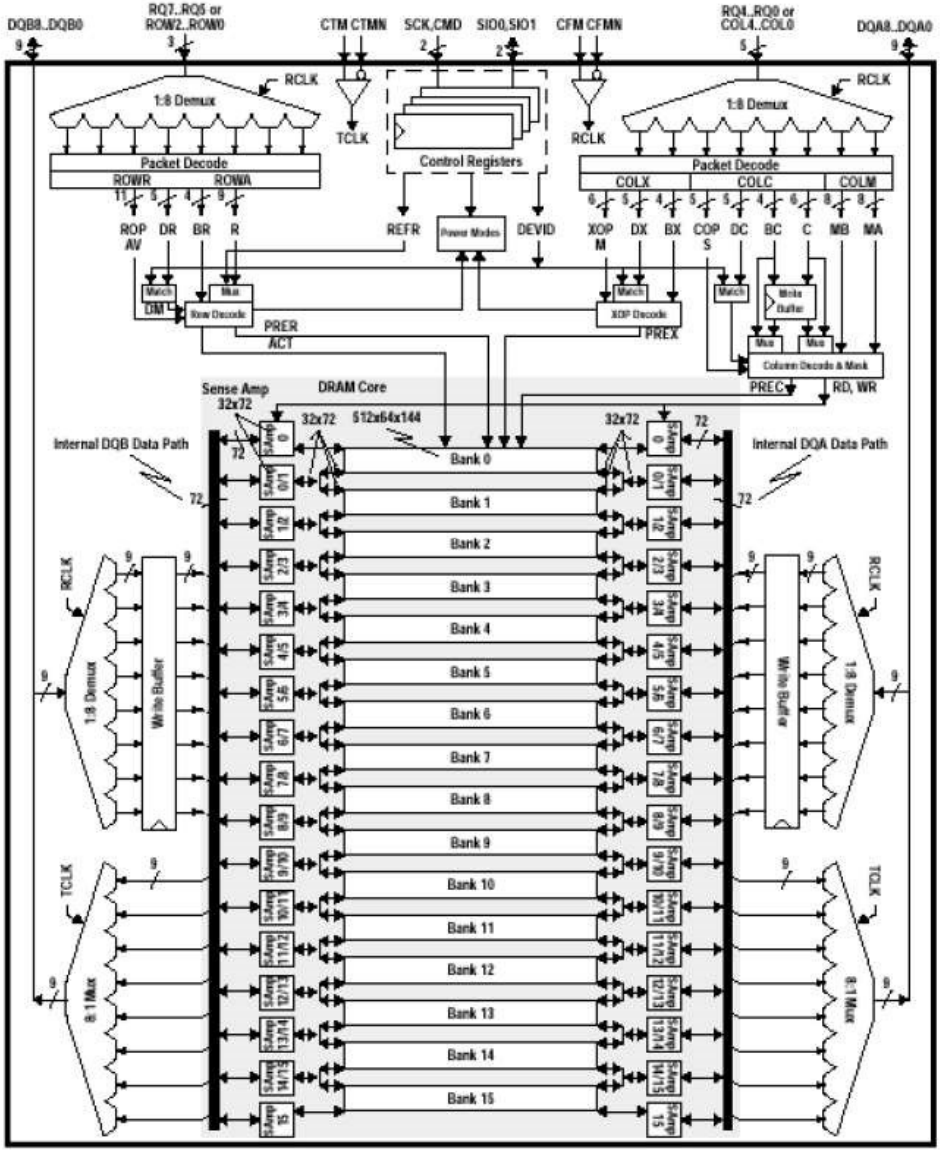
Modern DRAM

- SDRAM
  - synchronous, pipelined design
  - several banks
  - output delayed by multiple cycles
  - addressing similar to older DRAM
- RDRAM
  - Rambus DRAM
  - synchronous
  - many banks
  - packet switched internal network
  - low voltage signalling interface

Example SDRAM Timing



RDRAM Architecture



Example RDRAM Access